Student Number and Name :.....

ECE 476 MID-TERM EXAM **APRIL 22th, 2010-04-20**

4 questions. Total 100 points. Exam duration 2 hours. Open book, open notebook. No use of laptops, mobile phone or any wireless device. Print your name on every page.

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1. Two VHDL codes are given as (10p)

a.
```
SIGNAL Z, A, B, C, D: STD_LOGIC;
BEGIN
Z<=A AND B;
Z<=C OR D;
END BEHAVIOR;
```

b.
```
SIGNAL Z, A, B, C, D: STD_LOGIC;
BEGIN
PROCESS(A, B, C, D)
BEGIN
Z<=A AND B;
Z<=C OR D;
END PROCESS;
END BEHAVIOR;
```

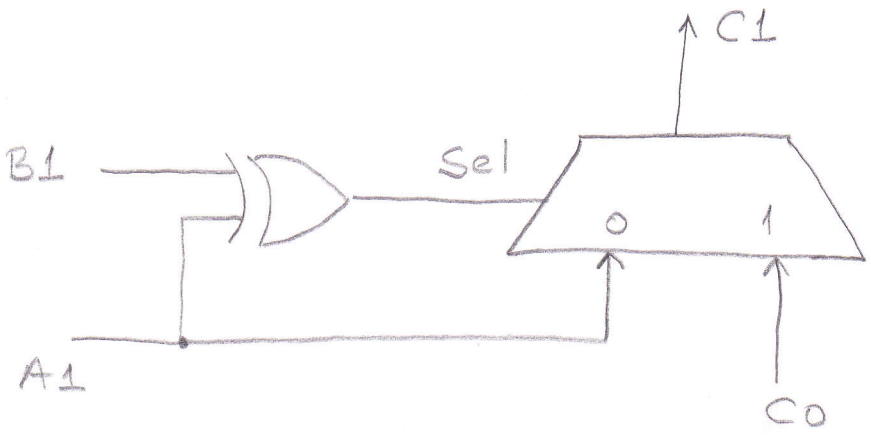
Show the corresponding logic circuits to these VHDL codes.

2. To prevent the ripple in the adders, a design can be made and used as shown below. The circuit immediately calculates the carry bit generated in a full adder. (40p)

a. Explain how this circuit calculates the carry bit.

b. Write all the the required VHDL codes to implement this circuit (A1, B1, C0 inputs, C1 output, all one-bit) by using the 2-to-1 mux as a component, using a concurrent conditional statement.

c. Write all the required VHDL codes to implement this circuit by using the 2-to-1 mux as a package, using a concurrent SELECT statement.



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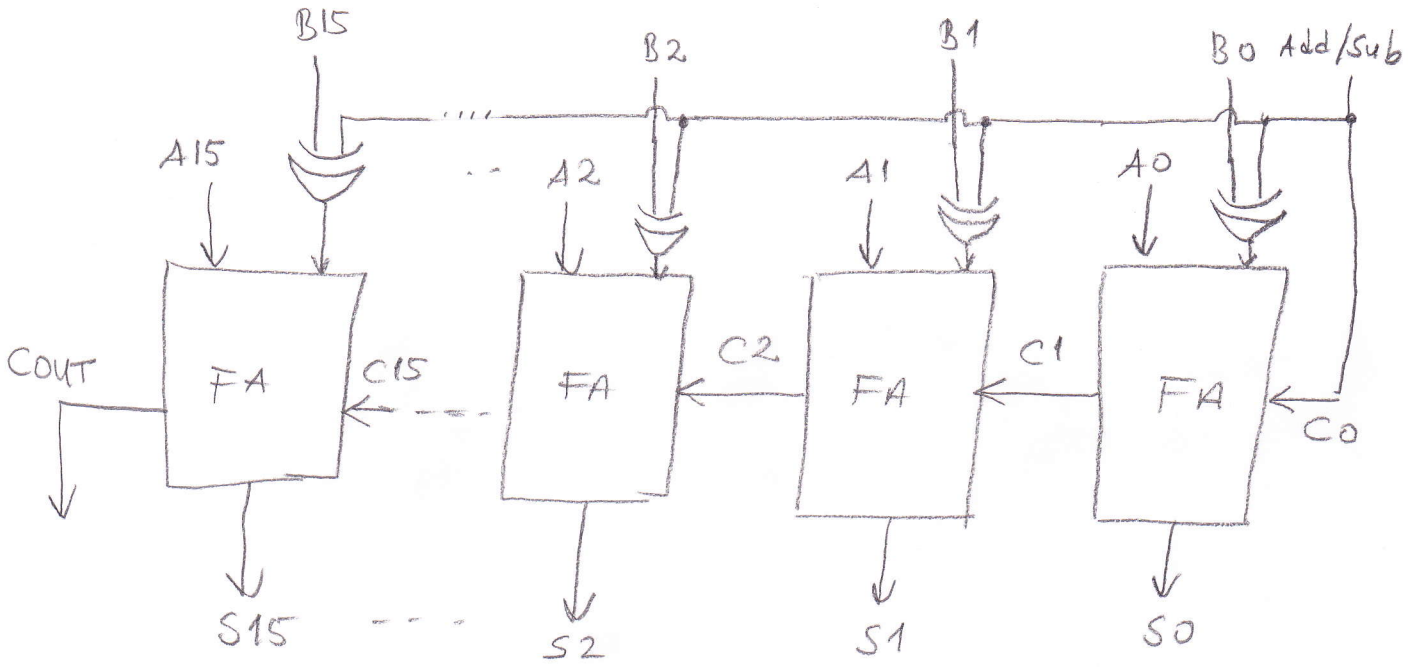
3. Provide the structural VHDL code for the circuit given below. (Use a 1-bit Full Adder (FA) as a package, and for-GENERATE statement in your code).(25p)



4. Consider an FPGA-operated heater shown below. This circuit is required to enable the ON/OFF control of the heater to adjust the temperature to a predefined temperature T_d. The desired control is such that the desired (T_d) and the measured (T_m) temperatures are converted into unsigned digital data of 4-bit and fed into the FPGA module. The FPGA outputs a control signal Y to control the heater such that the heater is turned on $(Y=1)$ when the measured temperature is lower than the desired, and turned off $(Y=0)$ otherwise. Provide the VHDL code of the circuit (use PROCESS statement in the coding).(25p)