ECE 476 FINAL EXAM 08 June 2010

Open book, open notebook. No laptop, wireless device or cellphone. There are 6 questions. Total 100 points. Write your number and name on every page. Duration 2.5 hours.

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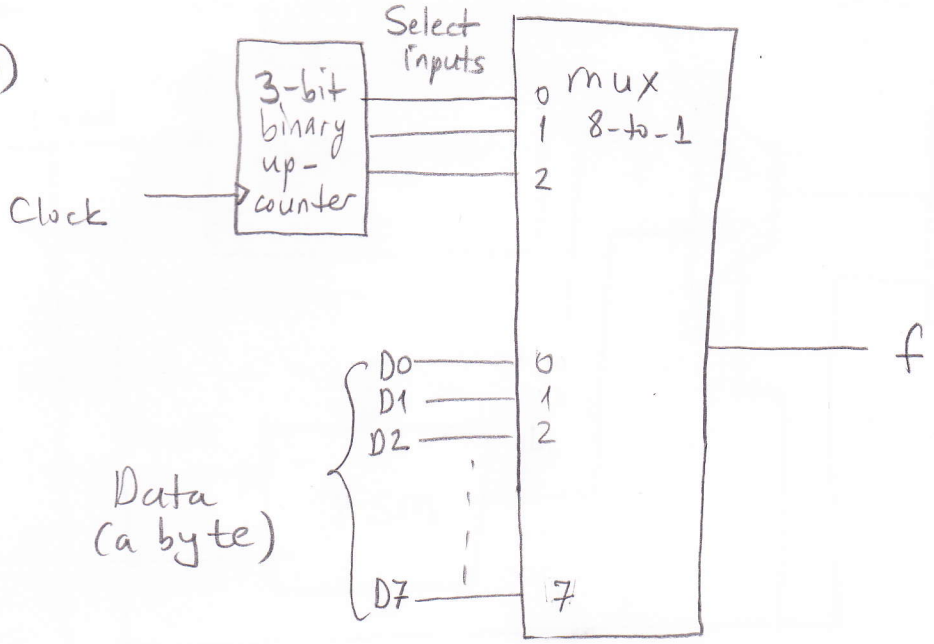
(1) (10p) Design a priority encoder of four inputs (r_3, r_2, r_1, r_0), r_3 having the highest and r_0 having the lowest priority, by using 2-to-1 multiplexers. Write the VHDL code of the circuit as well.

(2) (10p) Design a shifter circuit that can shift a four-bit input vector ($W_3 W_2 W_1 W_0$), one bit position to the right when the control signal Right=1, and one bit position to the left when Left=1. When Right = Left = 0, the output of the circuit should be the same as input vector W. When Right = Left = 1 the output shall be resetted (i.e., all zeroes). A zero should come for the rightmost and leftmost bit for shift left and shift right respectively.

a) Design the circuit,

b) Write the VHDL code.

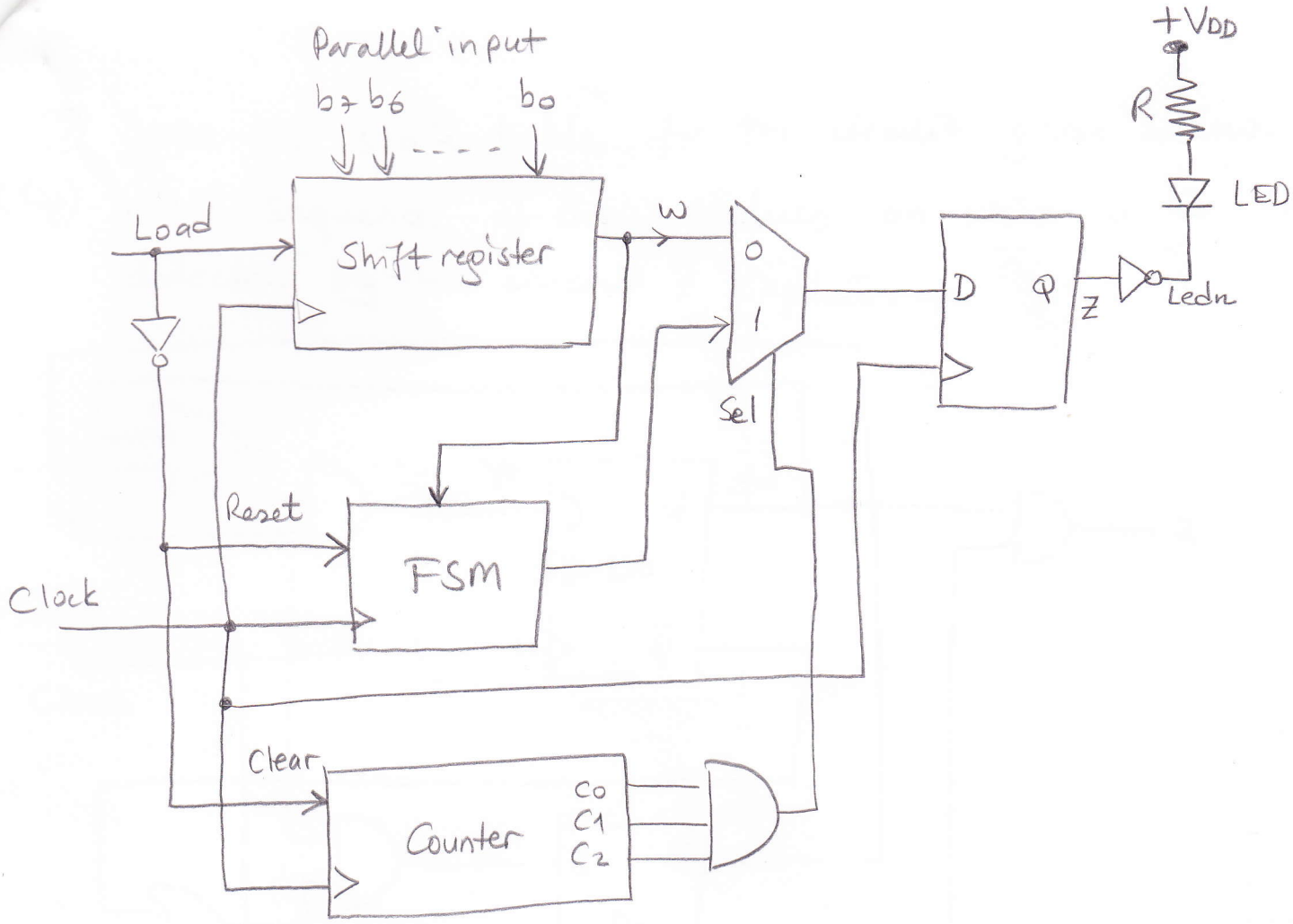
(3) (20p)



a) What do you think that the circuit performs? Explain.

b) Write the VHDL code for the circuit using the counter and the multiplexer as components (assume these components are given, use them in the main code only).

(4) (30p) Design a circuit that determines the even parity condition (even number of 1's) in a byte (8-bit input). The output z becomes 1 and a LED lamp is turned ON after 8-bit is count and the even parity condition is detected.

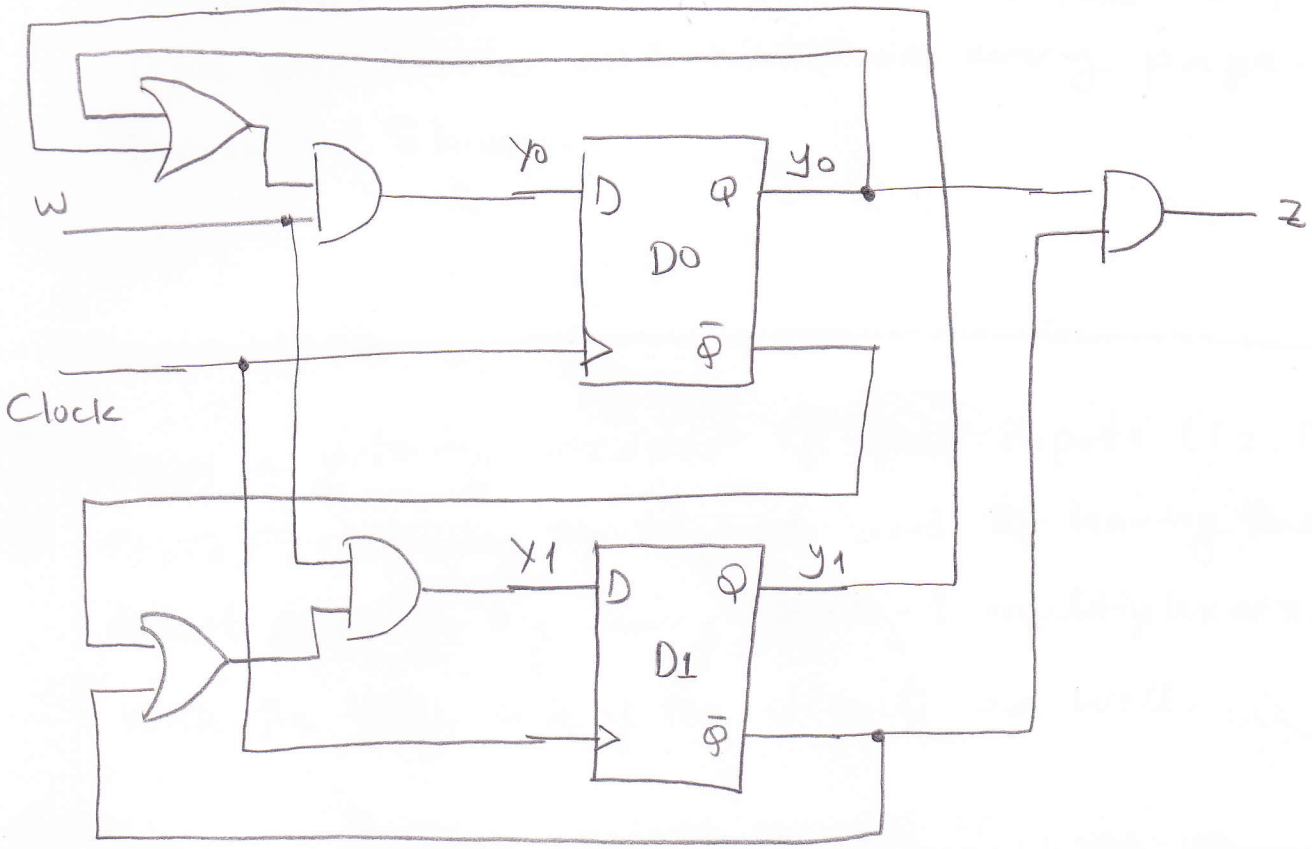


a) Design the FSM to detect the even number of the bits (b0 - - - b7) in the loaded byte into the parallel-load shift-register.

b) Write the VHDL codes for the shift register, the 3-bit binary up-counter, a 2-to-1 mux and a D FF as components.

c) Write the main VHDL code for the overall circuit to implement the functionality desired, using the components in the main code.

⑤ Derive the state table for the circuit given below.
(15p) What sequence of input values on wire w is detected by this circuit? Explain.



⑥ Design a counter that counts 0,1,2,3,0,1 (up)
(15p) when w=1, and 3,2,1,0,3 (down) when w=0. Write the VHDL code of the circuit.