ECE 476 MICROCOMPUTER ENGINEERING

FINAL EXAM. JUNE 10, 2009.

Open book. Duration 2.5 hours. There are 6 questions. Write your name on every page. Use the back of the pages for answers. Explain yourself clearly and work diligently.

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① Two VHDL codes are given as

a)
```
SIGNAL Z, A, B, C, D : std_logic ;
BEGIN
Z <= A AND B ;
Z <= C AND D ;
```

b)
```
SIGNAL Z, A, B, C, D : std_logic ;
BEGIN
PROCESS (A, B, C, D)
BEGIN
Z <= A AND B ;
Z <= C AND D ;
END PROCESS ;
```

Draw the corresponding logic circuits to these VHDL codes.

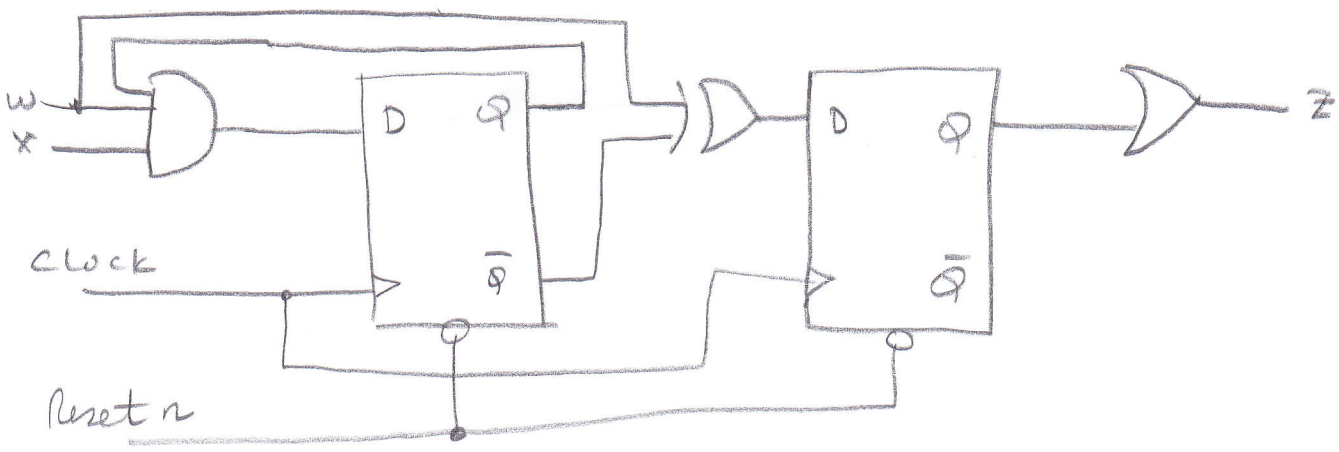
② a) Design a counter with T flip-flops and combinational circuit such that when Resetn = 0, it should asynchronously returns to "00" state; when Resetn = 1 it should count the sequence 00, 10, 01, 11, 00 --- when w = 1, and count the same sequence backwards (i.e., 00, 11, 01, 10, 00, 11 --) when w = 0.

b) Write the VHDL code for this finite state machine (FSM).

③ Develop and write the VHDL code for the FSM that detects the sequences 101 and 010 on the signal w. An example of the sequence and the output z is given as:

w :	0	0	0	0	1	0	1	1	0	1	0	1	1	0	0	1	0	1	0	0	0	0
z :	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	0	0	1	1	1	0	0

④ WRITE the VHDL code to implement the circuit

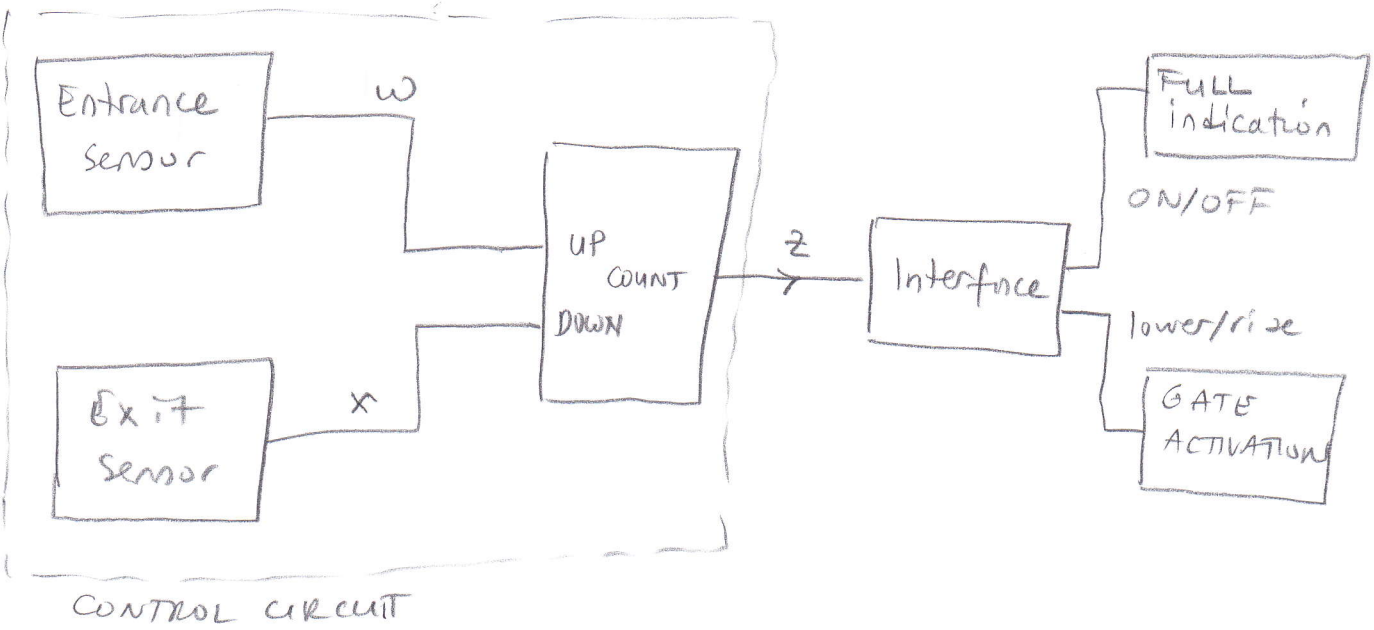


⑤ You want to monitor available spaces in a 100-space parking garage and you need to

- provide an indication of a FULL condition when there is no empty space by illuminating a display sign, and

- lowering a gate bar at the entrance when there are empty spaces available for an incoming car.

Functional block diagram of the monitoring circuit would be:



Assuming an entrance and exit do not occur at the same time,

a) Design the control circuit

b) Write the VHDL code for the control circuit

NOTE: Inputs are w, x, clock, Reset n
output is z (when z=1 garage is FULL, when z=0 the garage is empty (there are available spaces) and the gate bar can be lowered when there is an incoming car to park.

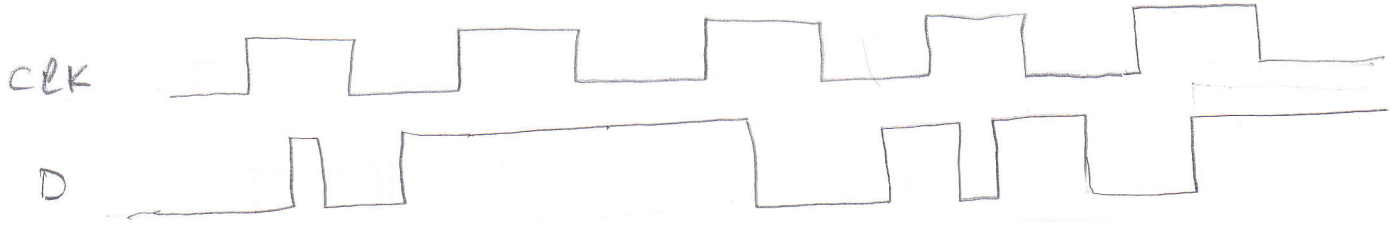
⑥ Two VHDL codes are given as

```
ENTITY CIRCUIT IS
PORT ( D, CLK : IN  STD_LOGIC;
       Q      : OUT STD_LOGIC);
END CIRCUIT
```

a)
```
ARCHITECTURE Behavior OF CIRCUIT IS
BEGIN
PROCESS (D, CLK)
BEGIN
 IF CLK = '1' THEN
     Q1 <= D;
 END IF;
 END PROCESS;
END Behavior;
```

b)
```
ARCHITECTURE Behavior OF CIRCUIT IS
BEGIN
PROCESS
BEGIN
WAIT UNTIL CLK'EVENT AND CLK = '0';
Q2 <= D;
END PROCESS;
END BEHAVIOR;
```

If we simulate and test the VHDL codes above, with the signals given below, draw Q1 and Q2



Q1 ----

Q2 ----