ECE 476 MIDTERM EXAM 15 April 2009

There are 6 questions. Open book. Duration 2 hours. Use the back of the page for answer. 100 points

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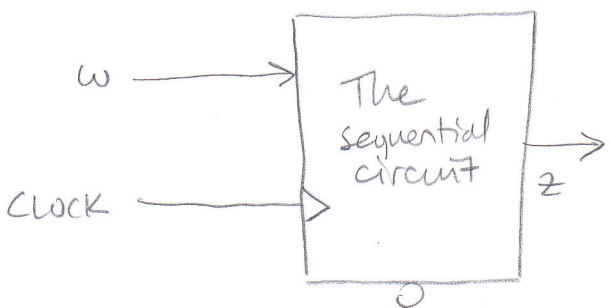
(1) (15p) Write the VHDL code for a circuit that routes the maximal value of three input signals (a, b, c) to the output (f). Write only the ARCHITECTURE portion of the code (Behavior). (input signals are not signed)

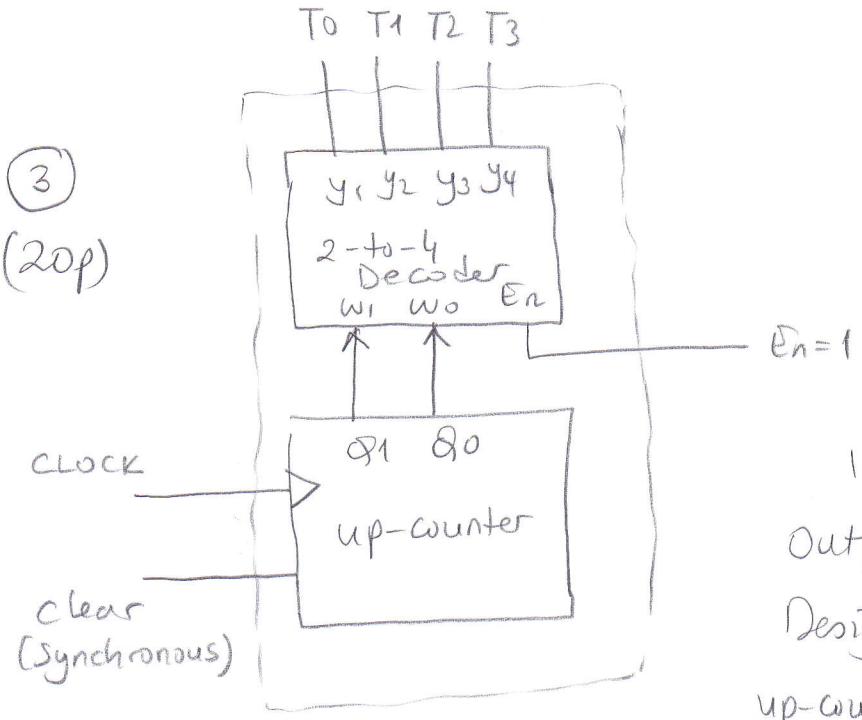
(2) (20p) a) Design a sequential circuit by using D flip flops and the required combinational logic circuit gates that detects two consecutive 1's in an incoming signal w. The output z will be 1 at the positive edge of the next clock cycle when two consecutive 1's occur in w. An example of sequence is given:

Clock :	t_0	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}
w :	0	1	0	1	1	0	1	1	1	0	1
z :	0	0	0	0	0	1	0	0	1	1	0



b) Write the VHDL code (structural) after your design

(3) (20p)



a) Explain what the circuit given here does.

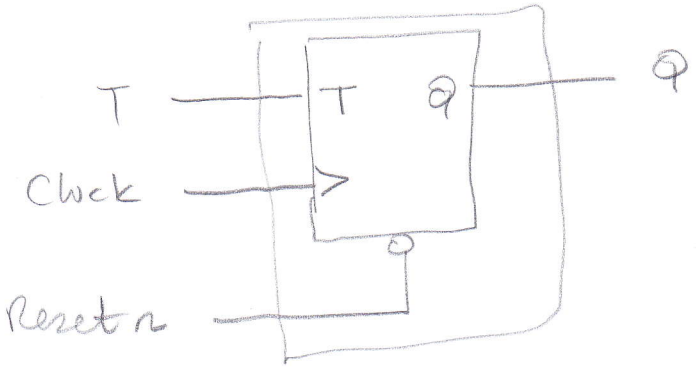
b) Write the VHDL code implementing the circuit.

Inputs are: clear, clock, En.

Outputs are: T0, T1, T2, T3.

Design the code such that up-counter and 2-to-4 decoder are used as components in the code. First write the VHDL code for the components (sub-circuits) in a component package, then use these components in the main code by package implementation

(4) (15p) Write the behavioral code for a T-flip flop with an asynchronous reset.



(5) (10p) Explain with an example why OVERFLOW occurs in SIGNED arithmetic and not occurs in UNSIGNED arithmetic. Show how the overflow condition is detected.

(6) (20p) a) Design a universal shift register (4-bit) with LOAD and CLEAR capability by using D-flip flops and 4-to-1 multiplexers. (Synchronous circuit)

S1	S0	Function	
0	0	Load Register	(R(0), R(1), R(2), R(3))
0	1	Shift Right	(w as an input from the left)
1	0	shift left	(w as an input from the right)
1	1	Load 0 (clear)	("0000")

b) Write the VHDL code to implement this circuit on an FPGA (Structural code).