ECE 477 LAB 9

1) In this lab, implementations are going to be transferred to an FPGA board. In this manner, GENESYS board, **Figure-1**, will be introduced first. Then the duty of "User Constraints File" will be explained. A simple example to use switches and LEDs on the FPGA board will be covered during the lab session.

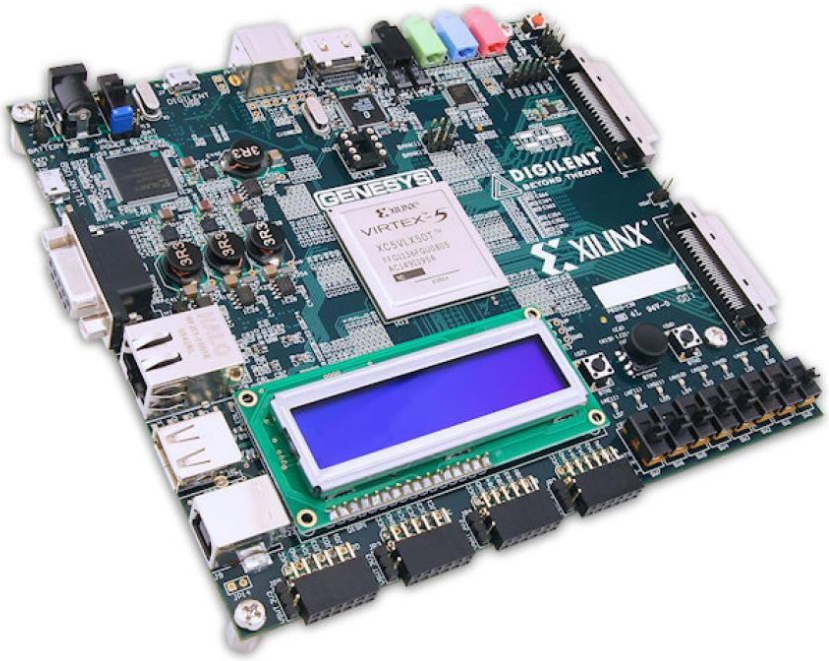


Figure-1 : Digilent Genesys Board

2) Implement a 3-to-8 Decoder in VHDL. See the results in the GENESYS board.

3) Write the VHDL code that describes a D flip-flop shown below **Figure-2**. Use a behavioral model in your description. Consider the R input to be and active-**low**, asynchronous input that resets the D flip-flop outputs when asserted. The sample code in **Figure-3** will guide you.

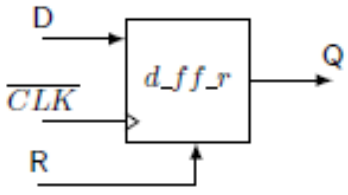


Figure-2 : A D flip-flop

```
-------------------------------------------------------------------
-- FET D Flip-flop model with active-high asynchronous reset input. --
-------------------------------------------------------------------
-- library declaration
library IEEE;
use IEEE.std_logic_1164.all;
-- entity
entity d_ff_r is
    port (   D,R :  in  std_logic;
             CLK :  in  std_logic;
               Q :  out std_logic);
end d_ff_r;
-- architecture
architecture my_d_ff_r of d_ff_r is
begin
   dff:  process (R,CLK)
   begin
      if (R = '1') then
         Q <= '0';
      elsif (falling_edge(CLK)) then
         Q <= D;
      end if;
   end process dff;
end my_d_ff_r;
```

Figure-3: D FF model with active-high asynchronous reset input

4) Write the VHDL code that describes a D flip-flop shown below **Figure-4**. Use a behavioral model in your description. Consider the S input to be and active-**low**, synchronous input that sets the D flip-flop outputs when asserted. The sample code in **Figure-5** will guide you.

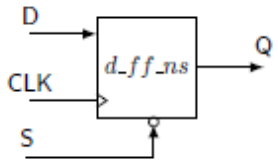


Figure-4 : A D flip-flop

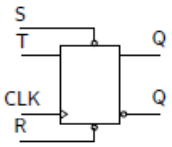
```
-- RET D Flip-flop model with active-low synchronous set input. --
-----------------------------------------------------------------
-- library declaration
library IEEE;
use IEEE.std_logic_1164.all;
-- entity
entity d_ff_ns is
    port (  D,S :  in  std_logic;
            CLK :  in  std_logic;
              Q :  out std_logic);
end d_ff_ns;
-- architecture
architecture my_d_ff_ns of d_ff_ns is
begin
   dff:  process (CLK)
   begin
      if (rising_edge(CLK)) then
         if (S = '0') then
            Q <= '1';
         else
            Q <= D;
         end if;
      end if;
   end process dff;
end my_d_ff_ns;
```

Figure-5: D FF model with active-low synchronous set input

Homework

1) Design a SR flip-flop with active-low synchronous reset.
2) Design a JK flip-flop with active-low asynchronous reset.
3) Design a T flip-flop with active-low synchronous reset.
4) Design a SR latch.
5) Below question.

EXERCISE 6. Provide a VHDL behavioral model of the T flip-flop shown on the right. The S and R inputs are an active low asynchronous preset and clear. Assume both the S and R inputs will never be asserted simultaneously.



Question for the group 5