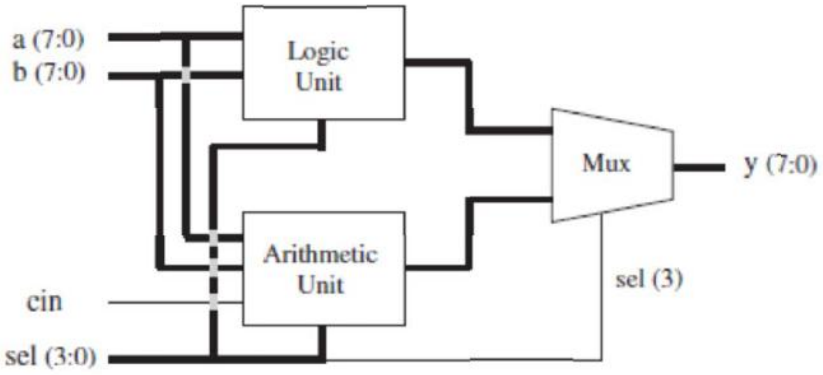
ECE 477 LAB 8

1) In the below figure a sample Arithmetic Logic Unit (ALU) and its truth table are presented. Write down the VHDL code of this ALU from the lecture notes and do related simulations.



sel	Operation	Function	Unit
0000	y <= a	Transfer a	Arithmetic
0001	y <= a+1	Increment a	
0010	y <= a-1	Decrement a	
0011	y <= b	Transfer b	
0100	y <= b+1	Increment b	
0101	y <= b-1	Decrement b	
0110	y <= a+b	Add a and b	
0111	y <= a+b+cin	Add a and b with carry	
1000	y <= NOT a	Complement a	Logic
1001	y <= NOT b	Complement b	
1010	y <= a AND b	AND	
1011	y <= a OR b	OR	
1100	y <= a NAND b	NAND	
1101	y <= a NOR b	NOR	
1110	y <= a XOR b	XOR	
1111	y <= a XNOR b	XNOR	

Figure-1 : An ALU design

2) Change the VHDL code of the previous question into a component style structure. RTL Schematic of the implementation should be seen like **Figure-1**. To check the implementation do related simulations.

3) Create a new project and do simulation in ISim Simulator. Explain its function.

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY COUNT_ONES IS
     GENERIC(N:INTEGER:=8);
    PORT ( INPUT_DATA : IN  STD_LOGIC_VECTOR (N-1 DOWNTO 0);
           ONES_NUMBER : OUT  INTEGER RANGE 0 TO N);
END COUNT_ONES;
```

```
ARCHITECTURE LOGIC_FLOW OF COUNT_ONES IS

BEGIN
    PROCESS (INPUT_DATA)
         VARIABLE TEMP: INTEGER RANGE 0 TO N;
         BEGIN
            TEMP := 0;
            FOR I IN 0 TO N-1 LOOP
                 IF (INPUT_DATA(I)='1') THEN
                      TEMP:= TEMP+1;
                 END IF;
            END LOOP;
          ONES_NUMBER <= TEMP;
    END PROCESS;
END LOGIC_FLOW;
```

Homework

No homework.