ECE 477 LAB 3

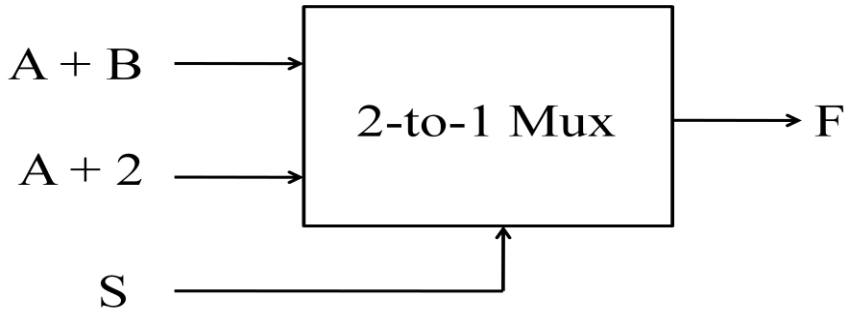
1) What is concatenation? Simulate below operations. A is two bit input, X and Y output.

X <= x"aa" & "10"&'1';

Y <= A & A & A & x"2B";

2) Addition in VHDL. ***Hint:*** *Add "use ieee.std_logic_arith.all;" and "use IEEE.STD_LOGIC_UNSIGNED.ALL;" in order to achieve summation and other arithmetic operations.*

3) Define A, B and S as inputs and F as output. Implement the circuit below. A and B are 4 bit numbers and F is five bit number.



Homework

1) Design a 1-to-2 Decoder with Enable. (Use logic gates)
2) Design a 2-to-4 Decoder with Enable. (Use "with-select")
3) Design a 3-to-8 Decoder with Enable. (Use "when-else")
4) Design a 4-to-16 Decoder with Enable. (Use "case")
5) Design an N-to-2^N Decoder with Enable. (Use "generic")