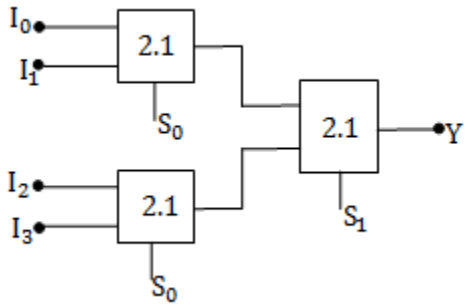
ECE 477 LAB 2

1) Construct 4 to 1 multiplexer in VHDL by using 2-to-1 multiplexers. 2-to-1 multiplexer should be constructed in a behavioral manner. Do related simulations. Inputs of the multiplexer are two bits numbers, 00, 01, 10 and 11.



http://www.vlsi-expert.com/2013/12/digital-basic-15-multiplexer-mux.html

2) Construct of 8 to 1 multiplexer in VHDL by using 4-to-1 multiplexers and 2-to-1 multiplexer. Do related simulations. Inputs of the multiplexer are three bits numbers; 000, 001,010, 011, 100, 101, 110 and 111.

Homework

1) Implement the function F(x,y,z,t)= ∑(0,4,6,8,11,12,15) by using 8-to-1 Mux and other logic gates. Use 8-to-1 multiplexer code in Q1 as a component. Solve the question on the paper then do the simulation on VHDL. Prepare a written report and deliver before the Labwork 3.