ECE 477 LAB 10

1) Open a new project in the ISE. Write down the example code, Leading zeros, from Lecture 9 page 6.

2) Open a new project in the ISE. Write down the example code, 0-to-7 Counter, from Lecture 10 page 7-8.

3) A clock divider will be introduced during the laboratory. Combine clock divider with previous question. Divide clock frequency of the Genesys board to 5 Hz. Show the result on the FPGA board.

Homework

1) 3 bit up counter with D flip flops(use DFF as component)
2) 3 bit down counter with D flip flops (use DFF as component)
3) Frequency divider with D flip flops (Divide 100 MHz to 25 MHz)
4) 3 bit down counter with T flip flop (use TFF as component)
5) 3 bit up counter with T flip flop (use TFF as component)