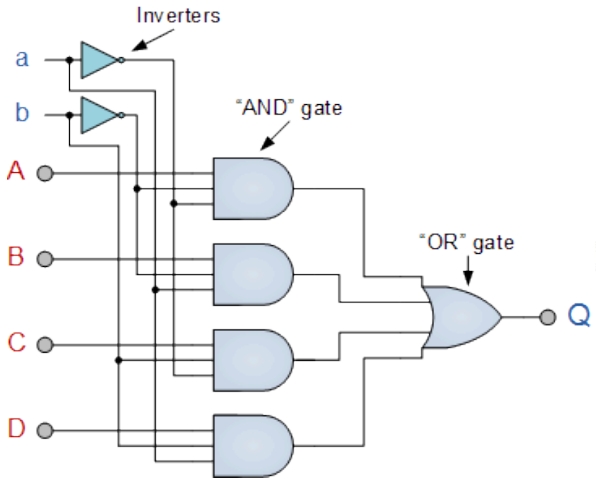
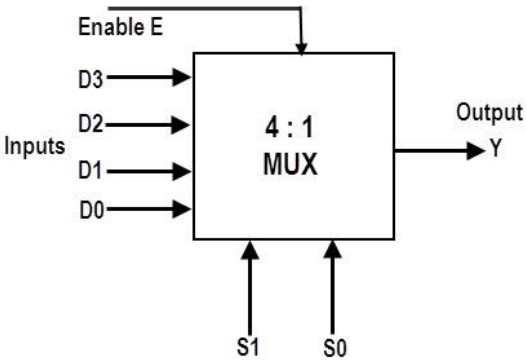
ECE 477 LAB 1

1) Construct 4 to 1 multiplexer in VHDL with inverters, AND and OR gates. Do related simulations. Inputs of the multiplexer are two bits numbers, 00, 01, 10 and 11.





http://www.electronics-tutorials.ws/combination/comb_2.html

http://www.electronicshub.org/multiplexerandmultiplexing/

2) Construct behavioral model of 4 to 1 multiplexer in VHDL. (Hand book page 125-126). Do related simulations. Inputs of the multiplexer are two bits numbers, 00, 01, 10 and 11.
3) How to use component in VHDL will be covered. Please, listen topic carefully. (Read Hand book page 201-219.)
4) Implement the function F(x,y,z)= ∑(1,2,3,5) by using 4-to-1 Mux and other logic gates. Use 4-to-1 Mux code as a component. Solve the question on the paper then do the simulation on VHDL.

Homework

1) Implement the function F(x,y,z,t)= ∑(1,2,3,5,11,12,13) by using 4-to-1 Mux and other logic gates. Use 4-to-1 Mux code as a component. Solve the question on the paper then do the simulation on VHDL.