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```
        ⋮

MUX2 : MUX4TO1 PORTMAP (W(4),W(5),W(6),W(7),
          S(1DOWNTO0), M(1));
MUX3 : MUX4TO1 PORTMAP (W(8),W(9),W(10),W(11),
          S(1DOWNTO0),M(2));
MUX4 : MUX4TO1 PORTMAP (W(12),W(13),W(14),W(15),
          S(1DOWNTO),M(3));
MUX5 : MUX4TO1 PORTMAP (M(0),M(1),M(2),M(3),
          S(3DOWNTO2),f);

END STRUCTURE;
```

VHDL CODE for a 16-to-1 mux by components

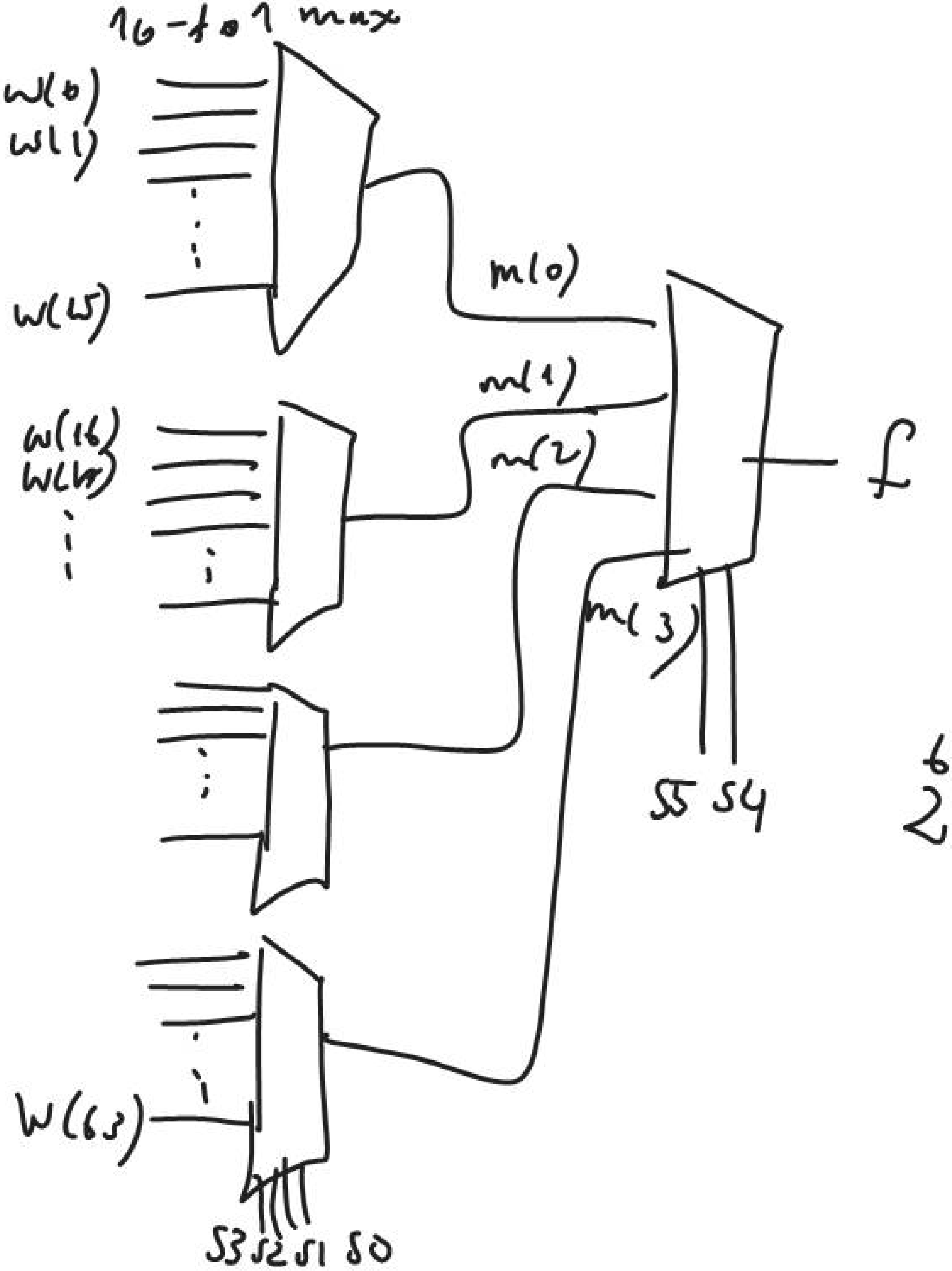
```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
ENTITY mux16to1 IS
PORT ( w : IN STD_LOGIC_VECTOR(0 TO 15);
       s : IN STD_LOGIC_VECTOR( 3 DOWNTO 0);
       f : OUT STD_LOGIC);
END mux16to1 ;
ARCHITECTURE Structure OF mux16to1 IS
SIGNAL m : STD_LOGIC_VECTOR(0 TO 3);
 COMPONENT mux4to1
  PORT ( w : IN STD_LOGIC_VECTOR (0 TO 3);
         s : IN STD_LOGIC_VECTOR (1 DOWNTO 0)
         f : OUT STD_LOGIC);
```

```
     END COMPONENT;

BEGIN

mux1: mux4to1  PORTMAP (w(0),w(1),w(2),w(3),
      s(1 DOWNTO 0), m(0));
    :
    :
    :
mux5: mux4to1 PORTMAP (m(0),m(1),m(2),m(3),
      s(3 DOWNTO 2), f);

END structure;
```



Lets design a 64to1 mux by using

4 16to1 mux + 1

4 to 1 mux

$64 = 2^6 = 2^4 . 2^2$

↓ ↓

16mux x4

$2^6 = 64$

A 16-TO-1 MUX WITH GENERATE CODE + PACKAGE

LIBRARY work;

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE work.mux4To1_package.all;
ENTITY mux n To 1 IS
* → GENERIC (n: INTEGER := 16);
PORT (w : IN STD_LOGIC_VECTOR(0 TO n-1);
      s : IN STD_LOGIC_VECTOR(n/4-1 DOWNTO 0);
      f : OUT STD_LOGIC);
END mux n To 1;

ARCHITECTURE STRUCTURE OF muxnto1 IS
SIGNAL m : STD_LOGIC_VECTOR(0 TO 3);
BEGIN
```

n÷4-1

Generate Loop

```
G1 : FOR i IN 0 TO n/4-1 GENERATE

MUXES : muxn/4 TO 1 PORTMAP ( W (n/4*i),
W( n/4 *i+1), W( n/4*i+2), W( n/4*i+3), S(n/4-1
DOWN TO 0), m(i)) ;
END GENERATE ;

mux 5 : mux4 TO 1 PORTMAP ( m(0), m(1), m(2),
m(3), S(n/4+1 DOWNTO n/4 ), f) ;

END STRUCTURE;
```