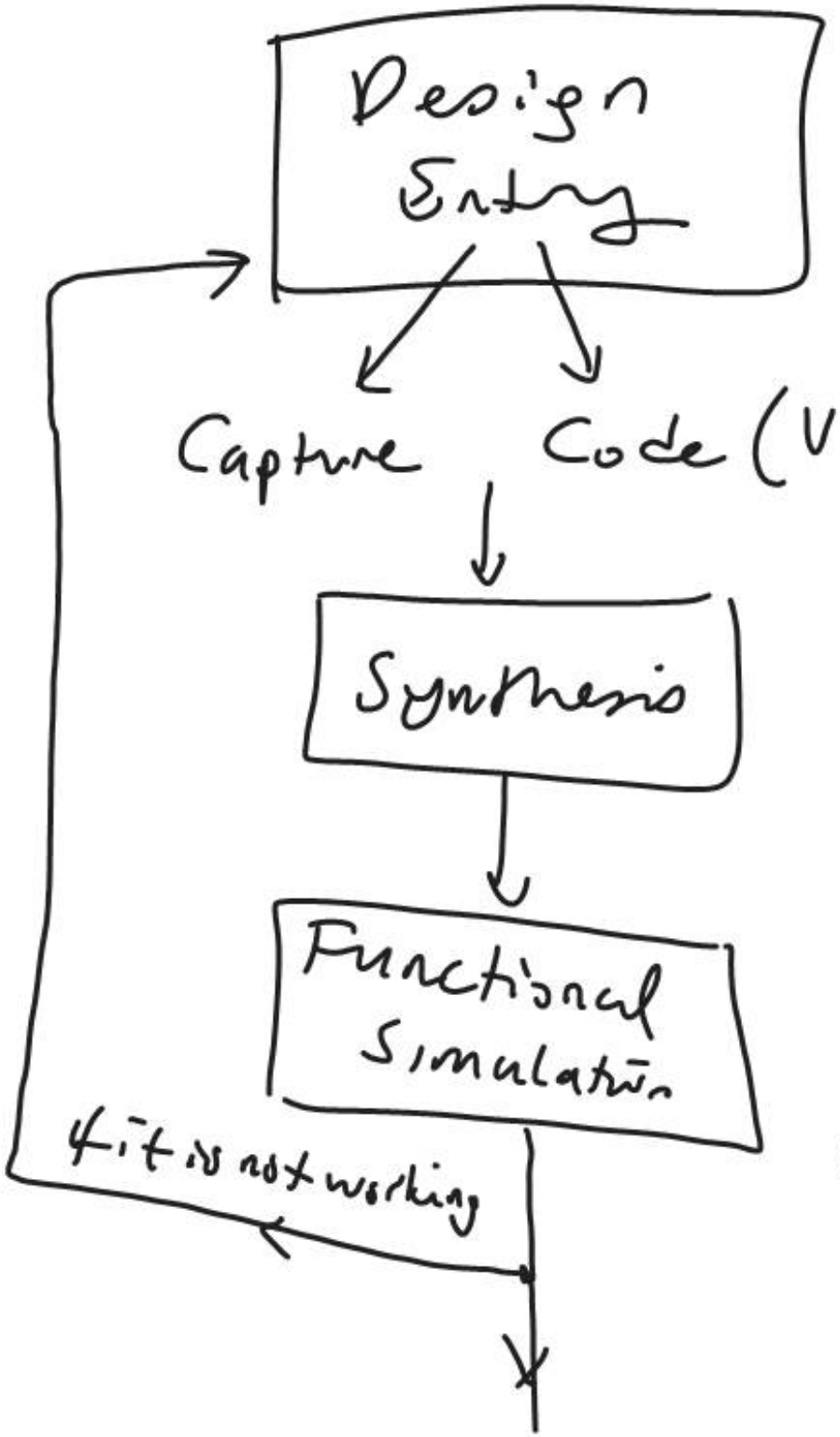

21.02.2011

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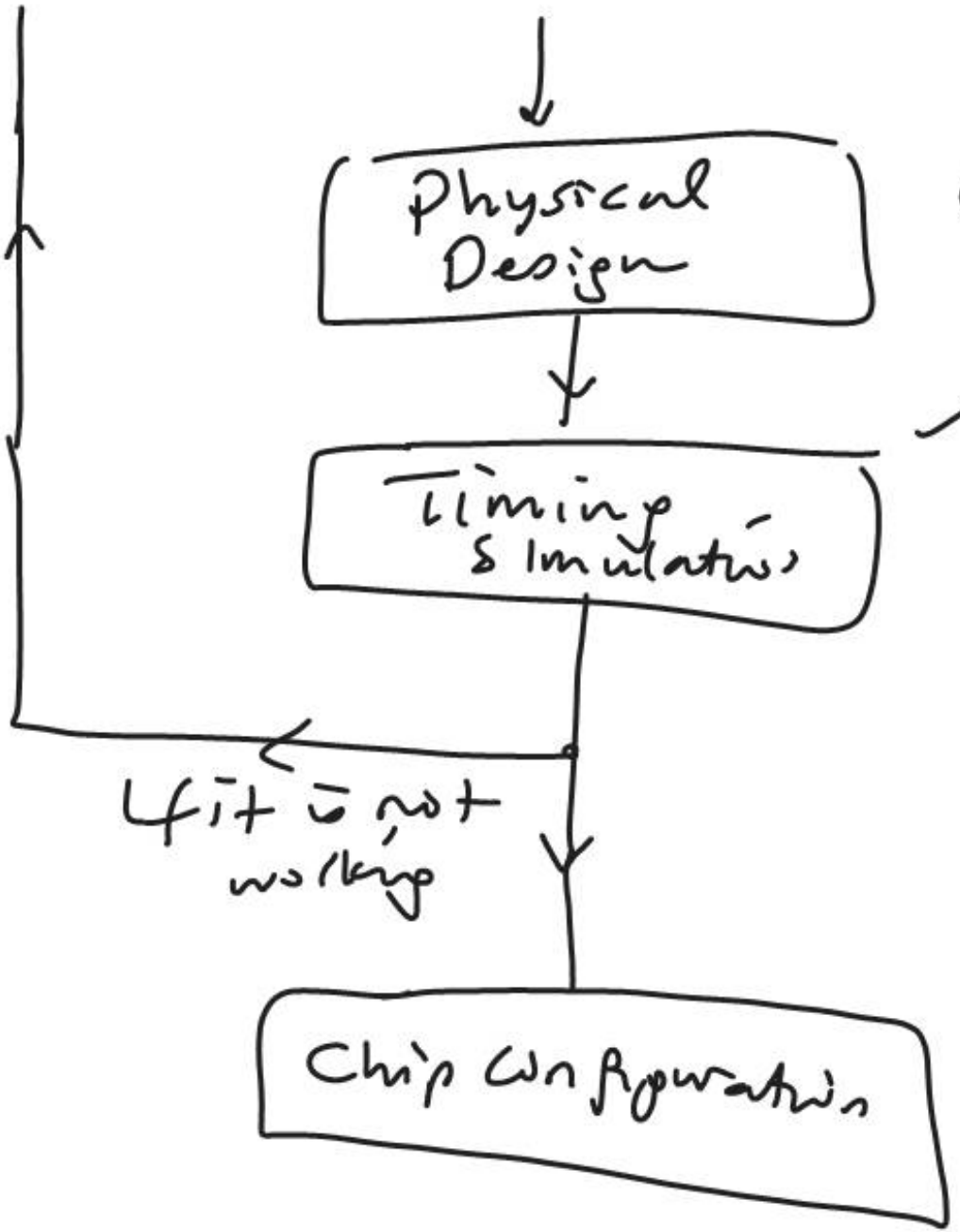
Tools (CAD Tools)

Logical codes are generated (netlist)

CAD Tool

Gates are ideal $t_{pH}=0$

There is no wire delay



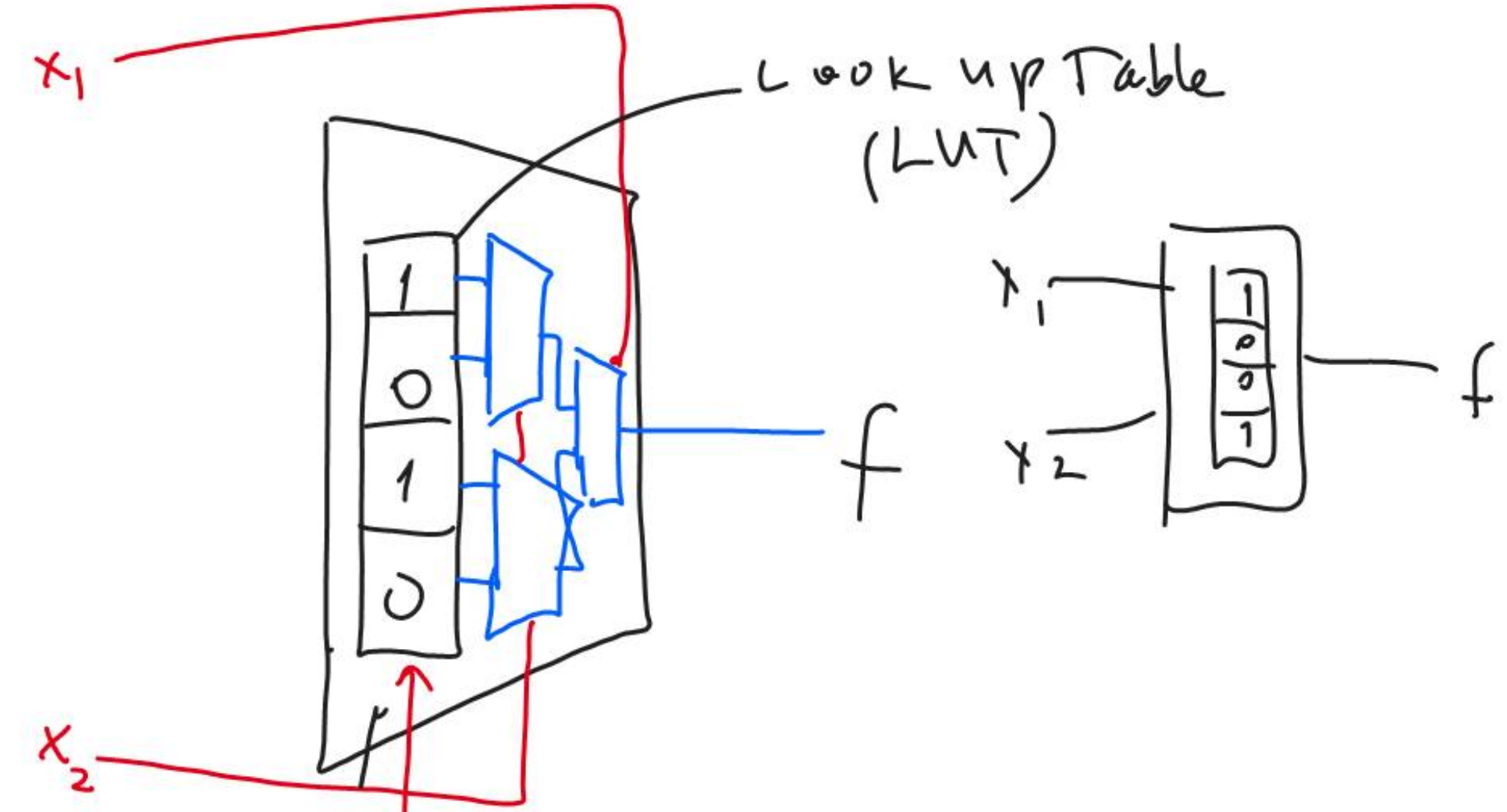
CAD Tool
Gates have tpit
wires have delay

Circuit design is implemented on the FPGA or CPLD etc.
and Tested again

CPLD
PAL
PLA
} based on NMOSs and In EEPROM structure (not volatile)

FPGA ⇒ based on SRAMs (Static RAMs)

They are volatile



Truth Table

x_1	x_2	f
0	0	1
0	1	0
1	0	0
1	1	x