



ARCHITECTURE Structure of adder is

SIGNAL C : STD\_LOGIC\_VECTOR(1 to 3);

BEGIN

Stage 0: fulladd PORTMAP ( Cin, X(0), Y(0), S(0), C(1));

Stage 1: fulladd PORTMAP ( C(1), X(1), Y(1), S(1), C(2));

Stage 2: fulladd PORTMAP ( C(2), X(2), Y(2), S(2), C(3));

Stage 3: fulladd PORTMAP ( C(3), X(3), Y(3), S(3), Cout);

END Structure;

# Adder

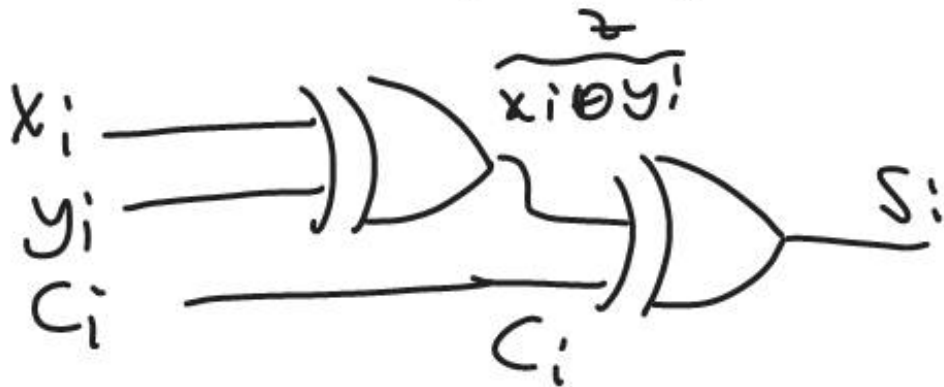
$$X + Y = S$$

STRUCTURAL WAY:

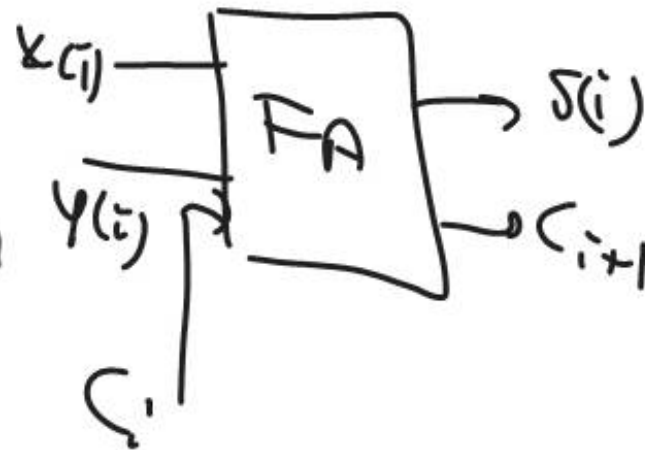
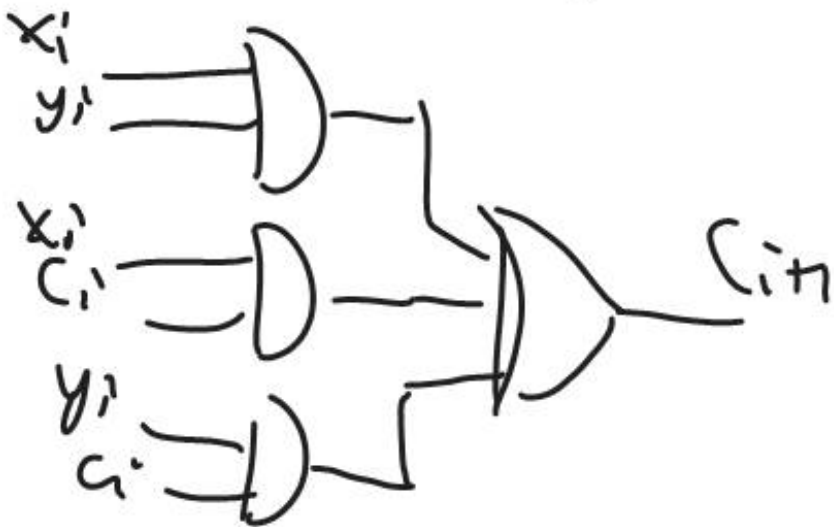
$$X(i) \oplus Y(i) \oplus C_i = S_i$$

It is possible to do the same thing with

$$(X(i) \text{ AND } Y(i)) \text{ OR } (X(i) \text{ AND } C_i) \text{ OR } (Y(i) \text{ AND } C_i) = C_{i+1}$$



ARITHMETIC STATEMENTS  
~~Behavioral~~  
 $(x_i \oplus y_i) \oplus C_i = x_i \oplus y_i \oplus C_i$



It is possible to DESIGN ENTRY with  
ARITHMETIC STATEMENTS

Arithmetic  $\begin{cases} \rightarrow$  signed numbers \\ \rightarrow unsigned numbers

$\Rightarrow$  `ieee.std_logic_signed.ALL;`

Then we can use arithmetic statements

`USE ieee.std_logic_arith.ALL;`

this way we can do arithmetic with  
 $\left. \begin{array}{l} \text{- signed} \\ \text{- unsigned} \end{array} \right\} \text{ numbers.}$

# ARITHMETIC ASSIGNMENT STATEMENTS

ex: LIBRARY ieee;

USE ieee.std\_logic\_1164.all;

USE ieee.std\_logic\_signed.all;

ENTITY Adder16 IS

PORT (X, Y: IN STD\_LOGIC\_VECTOR (15 DOWNTO 0);

S: OUT STD\_LOGIC\_VECTOR (15 DOWNTO 0);

END Adder16;

ARCHITECTURE Behavior of Adder16 IS

BEGIN

S <= X + Y;

END BEHAVIOR;

(no carry out, no overflow)  
carry in

to consider carries and overflow:

⋮  
USF ieee\_std\_logic\_signed\_all;

ENTRY Addr 16 LS

PORT ( X, Y : IN STD\_LOGIC\_VECTOR(<sup>16-bit</sup>LS DOWN TO 0));

    Cin : IN STD\_LOGIC;

    S : OUT STD\_LOGIC\_VECTOR(LS DOWN TO 0);

    Cout, overflow : OUT STD\_LOGIC);

END Addr 16;

ARCHITECTURE Behavior Addr 16 IS

SIGNAL sum : STD\_LOGIC\_VECTOR(16 DOWN TO 0);  
<sup>17-bit</sup>

BEGIN

$SUM \leftarrow \underline{(X \oplus Y)} + Y + C_{in}; (?)$

17 bit

16 bits

$S \leftarrow SUM(15 \text{ DOWN TO } 0);$

$C_{out} \leftarrow SUM(16);$

$OVERFLOW \leftarrow SUM(16) \oplus X(15) \oplus Y(15) \oplus R$

END BEHAVIOR;  $C_n \oplus C_{n-1}$   $C_{n-1}$   $SUM(15)$







# SIGNED NUMBERS

$$n = 4$$

ex  $0101 = x$   
          +5

$$x * 2 = 01010_{10} \checkmark$$

8    2

ex  $y = 1100_{-4}$

$$y * 2 = 11000_{-8}$$

Divide by 2

ex  $x = 0110_b$

$$0011 = x \div 2$$

3

$$y = 1100_{-4}$$

$$\begin{array}{r} 0100 \\ \underline{0101} \\ 5 \end{array}$$

$$y \div 2 = 110_{-2}$$

$$\begin{array}{r} 0011 \\ \underline{0100} \\ -4 \end{array}$$

$$\begin{array}{r} 0001 \\ \underline{0100} \\ -2 \end{array}$$

-2

Multiply by  $2^k$  is done by shifting left by  $k$  times.

ex 4-bit numbers

$M \Rightarrow 0111$  multiplicand  $m_3 m_2 m_1 m_0$

$Q \Rightarrow 0101$  multiplier  $q_3 q_2 q_1 q_0$

$q_0 = 1$

$p_0$

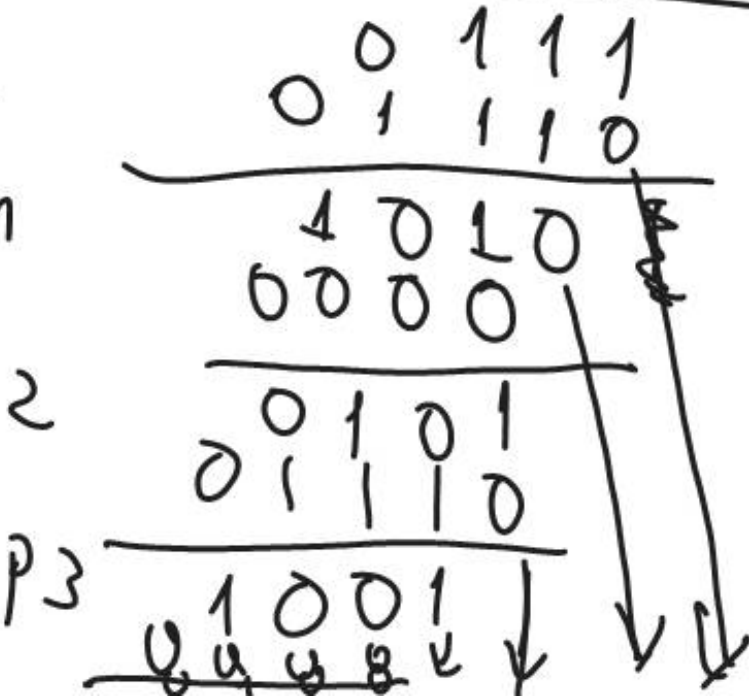
$q_1 = 0$

$p_1$

$q_2$

$p_2$

$q_3$



Product

01001101

~~X~~