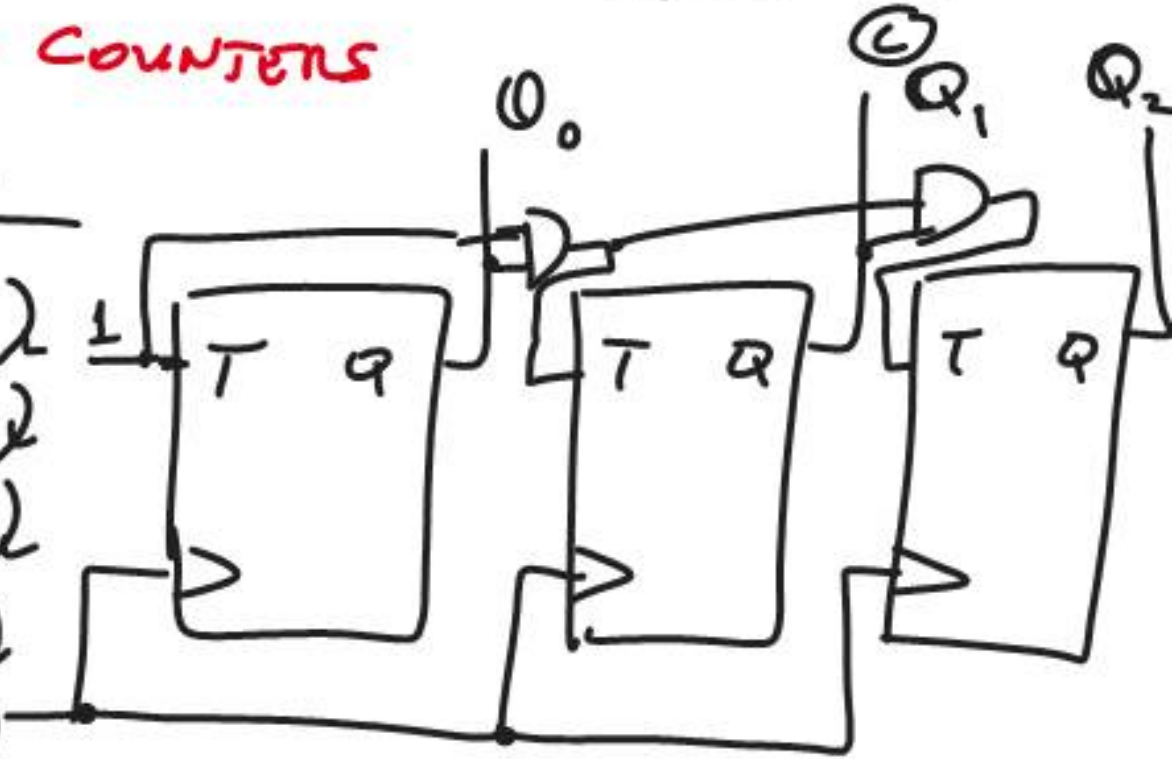
18.04.2011

SYNCHRONOUS COUNTERS

Clock Cycle	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
0	0	0	0



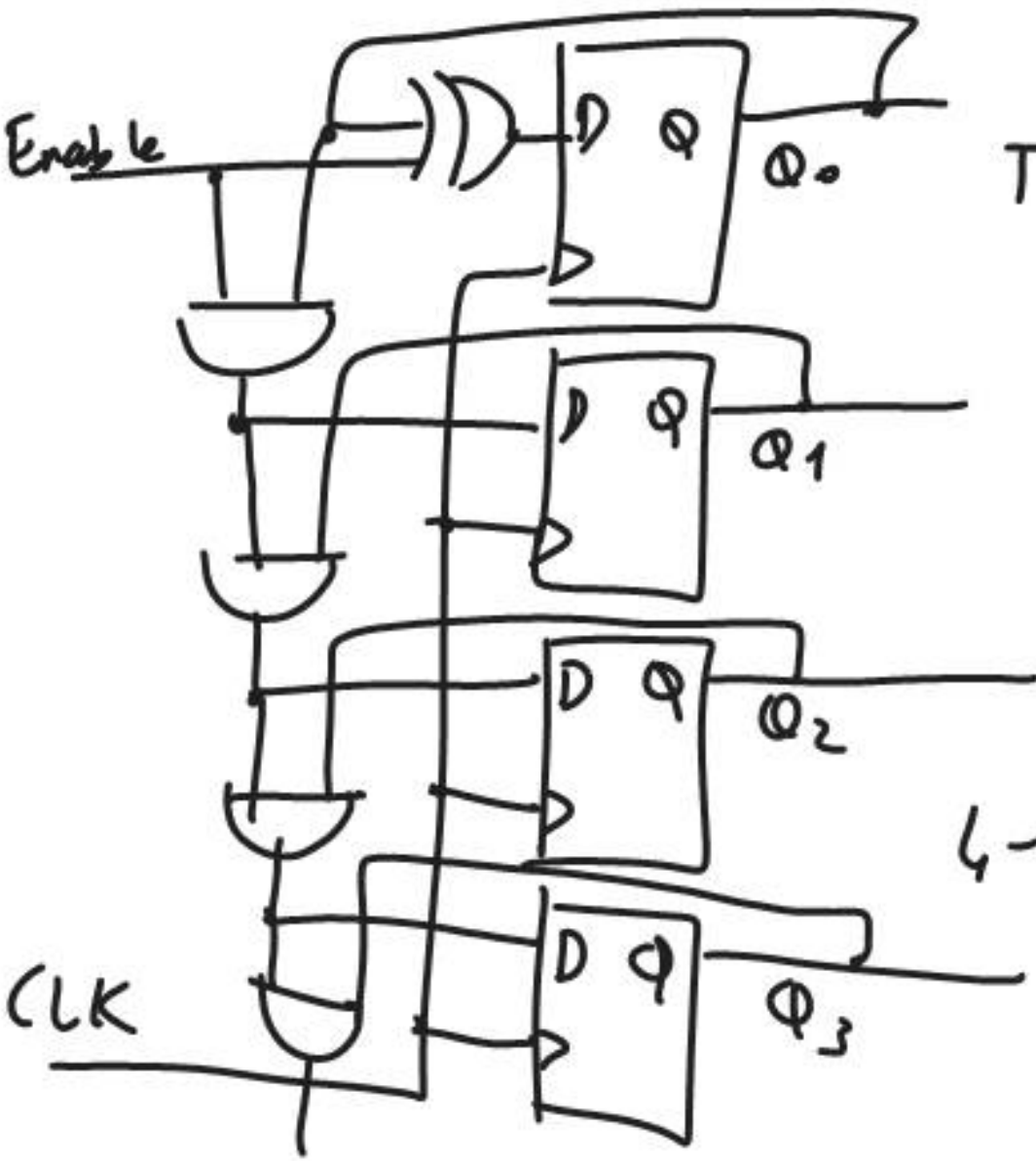
$T_0 = 1$

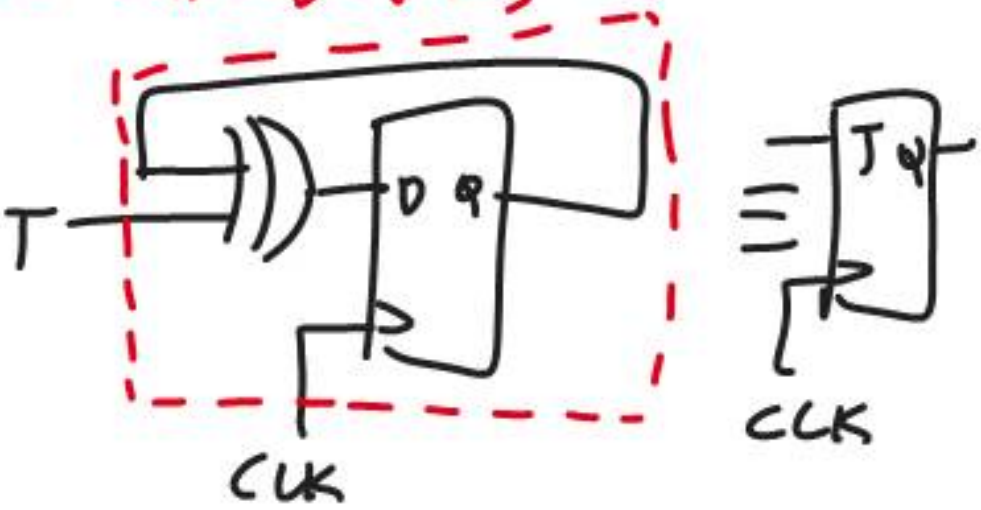
$T_1 = Q_0 \cdot 1$

$T_2 = Q_1 \cdot Q_0 \cdot 1$

synchronous binary up counter

Synchronous up-counter with D-FFs





fanout: #of gates a gate can drive.

4-bit binary counter with 0 FFs.

$D_0 = Q_0 \oplus Enable$

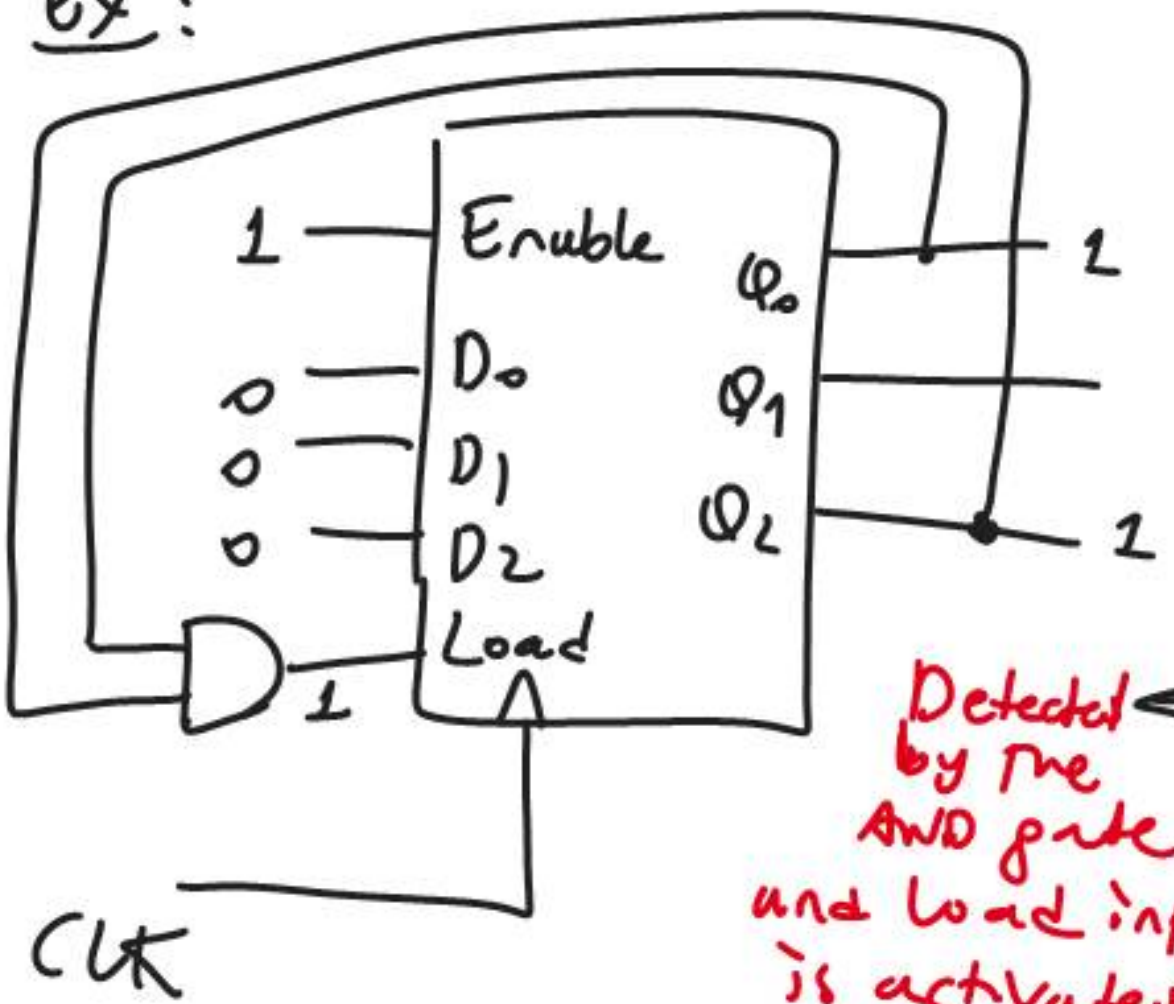
$D_1 = Q_1 \oplus Q_0 \cdot Enable$

$D2 = Q_2 \oplus Q_1 Q_0 \cdot Enable$

$D3 = D_3 \oplus Q_2 Q_1 Q_0 - -$

Normally in a Finite State Machine (FSM, a counter is an FSM) the FF inputs for the next states are calculated

Ex:

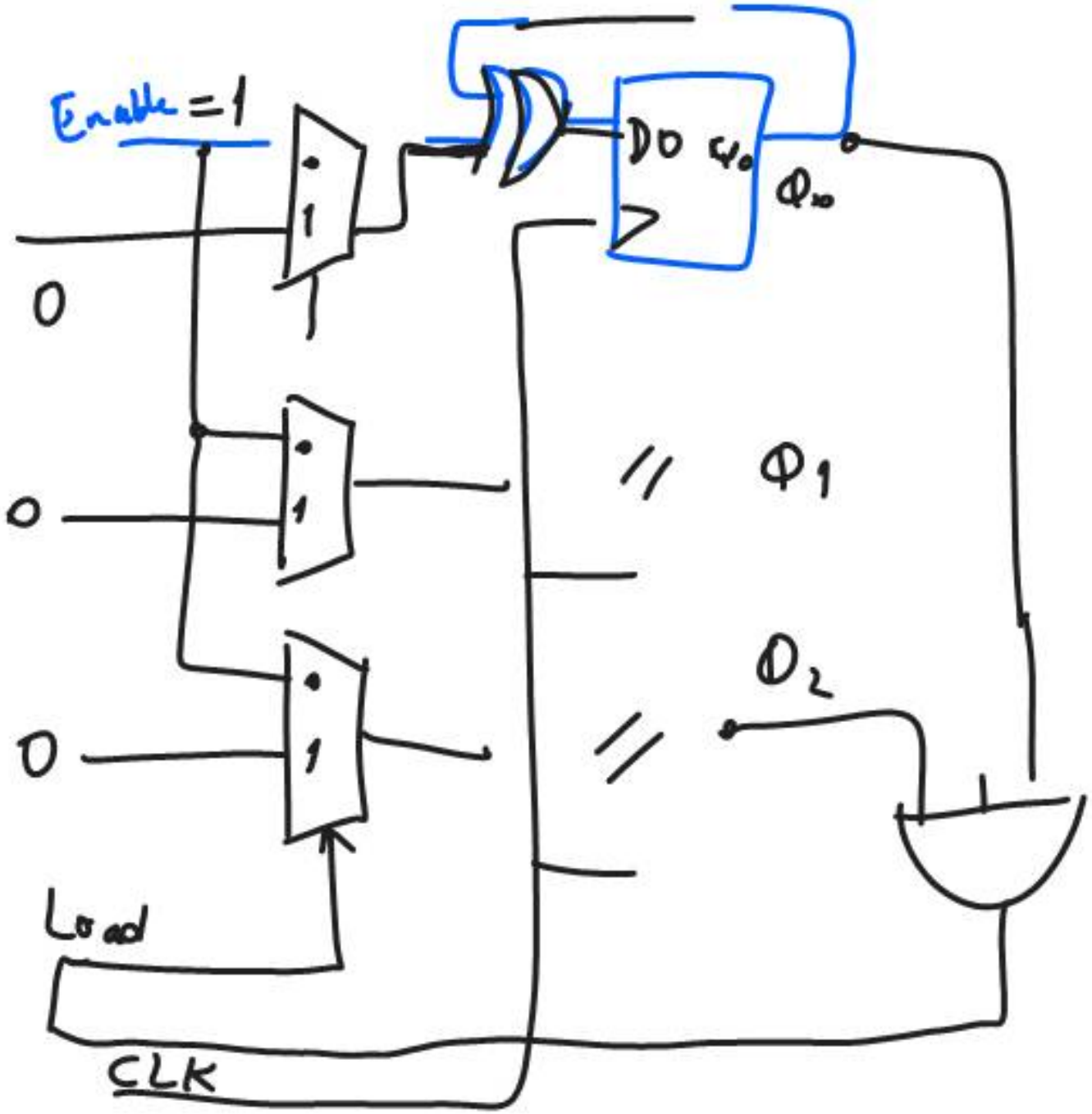


A modulo 6 counter:

Q_2 Q_1 Q_0
0 0 0
0 0 1
0 1 0
0 1 1
1 0 0
1 0 1
0 0 0

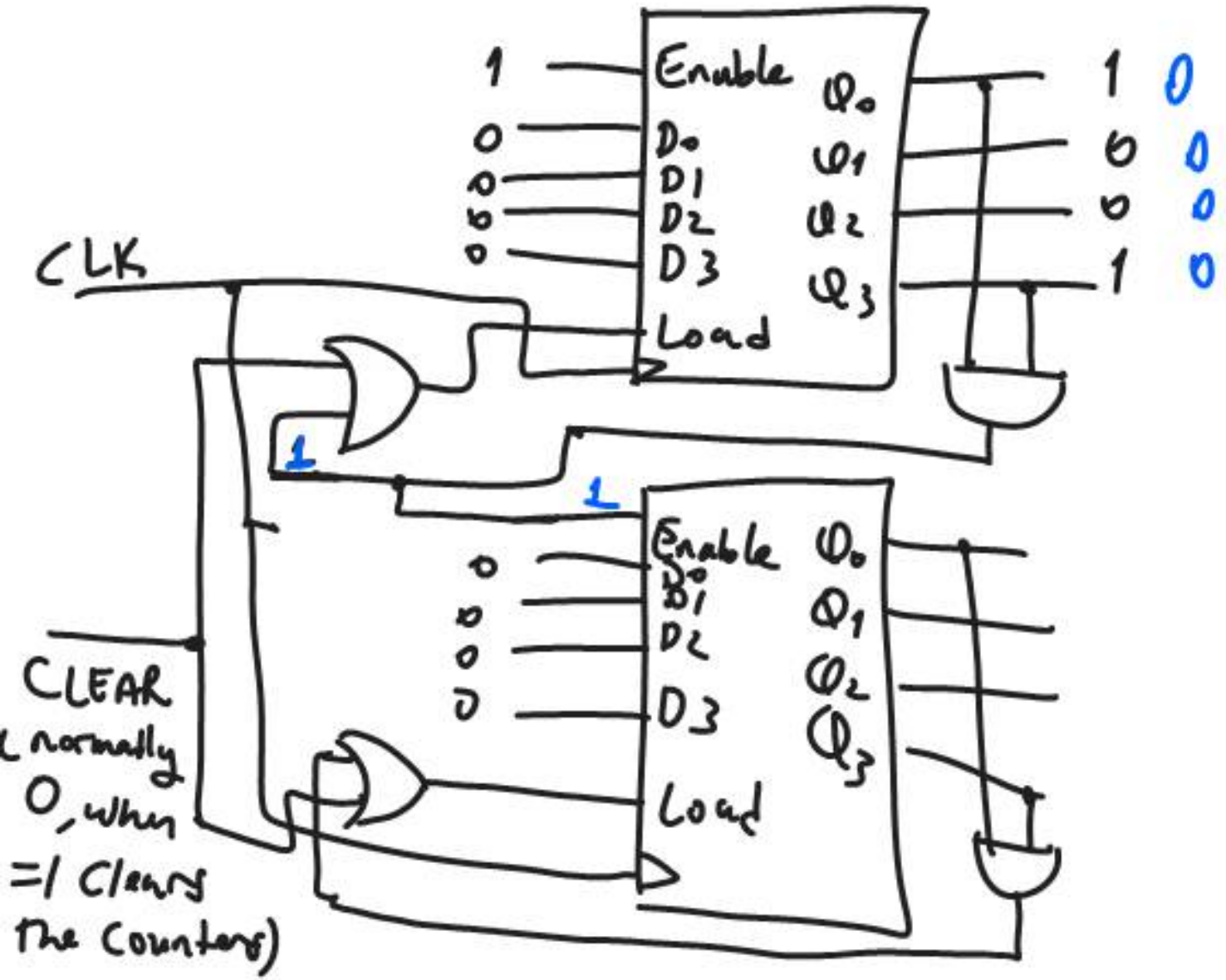
Detected by the AND gate and load input is activated

This is loaded into the D FFs



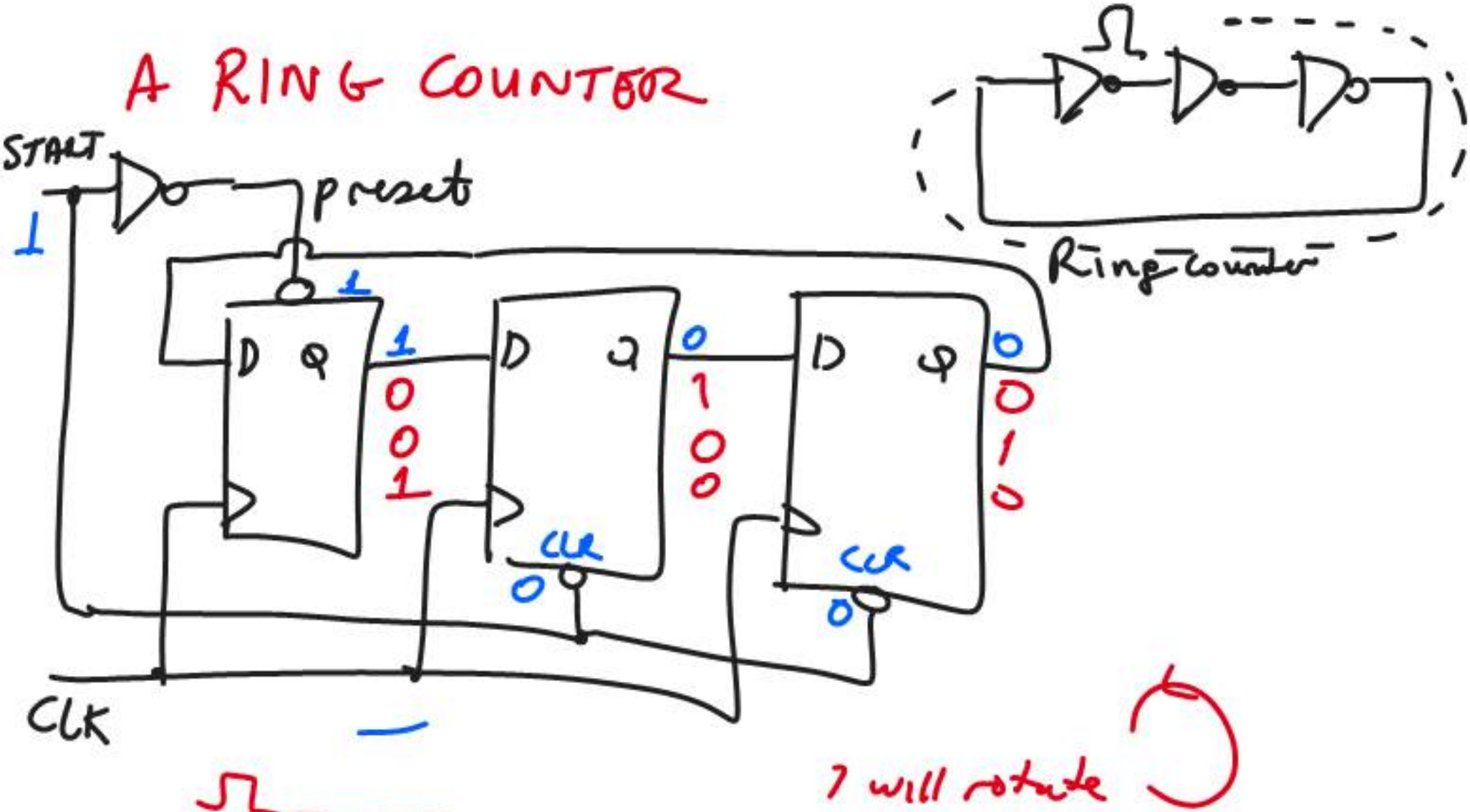
Inside of the previous modulo-6 counter

ex: A BCD Counter (2 digits)



B_2	B_1	B_0	DECIMAL
0	0	0	
		⋮	
0	0	9	
0	1	0	
0	1	1	
0	1	2	
0	1	3	
0	1	4	
		⋮	
0	1	9	
0	2	0	
		⋮	
0	9	9	
1	0	0	

A RING COUNTER



A Four-bit ring Counter