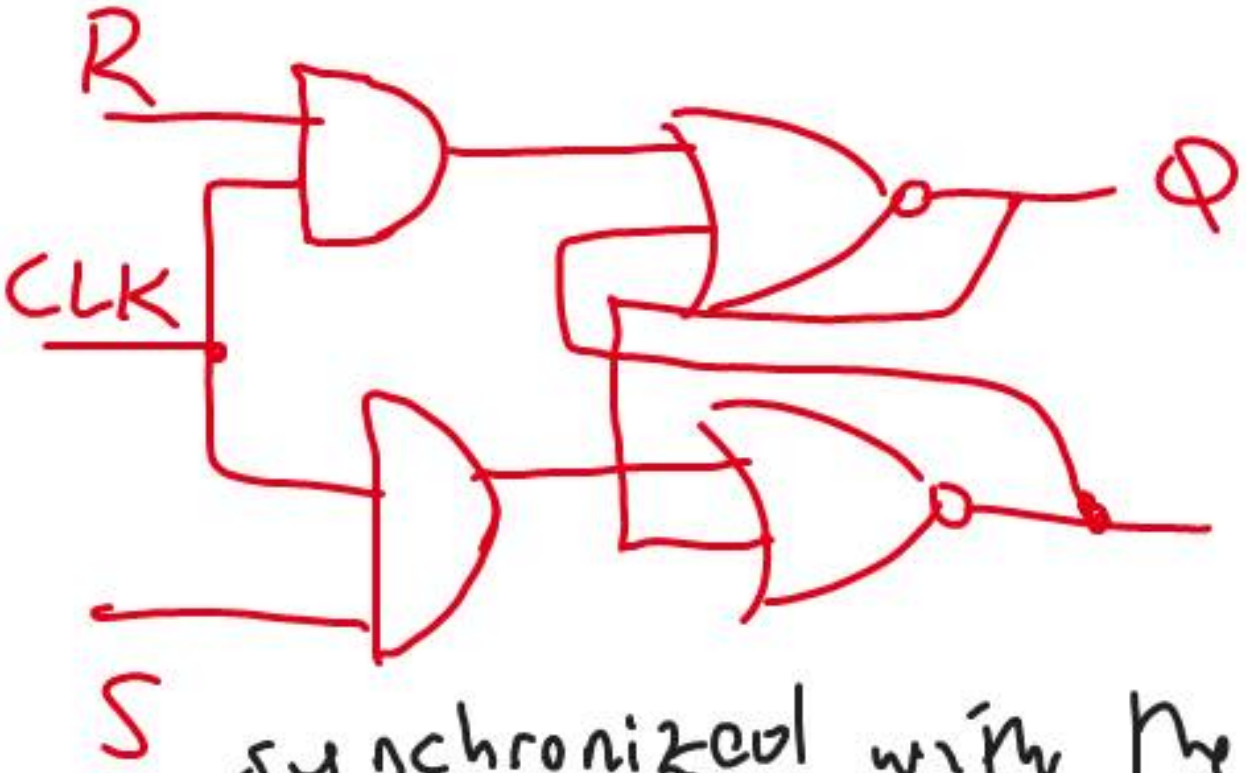
SR LATCH GATED

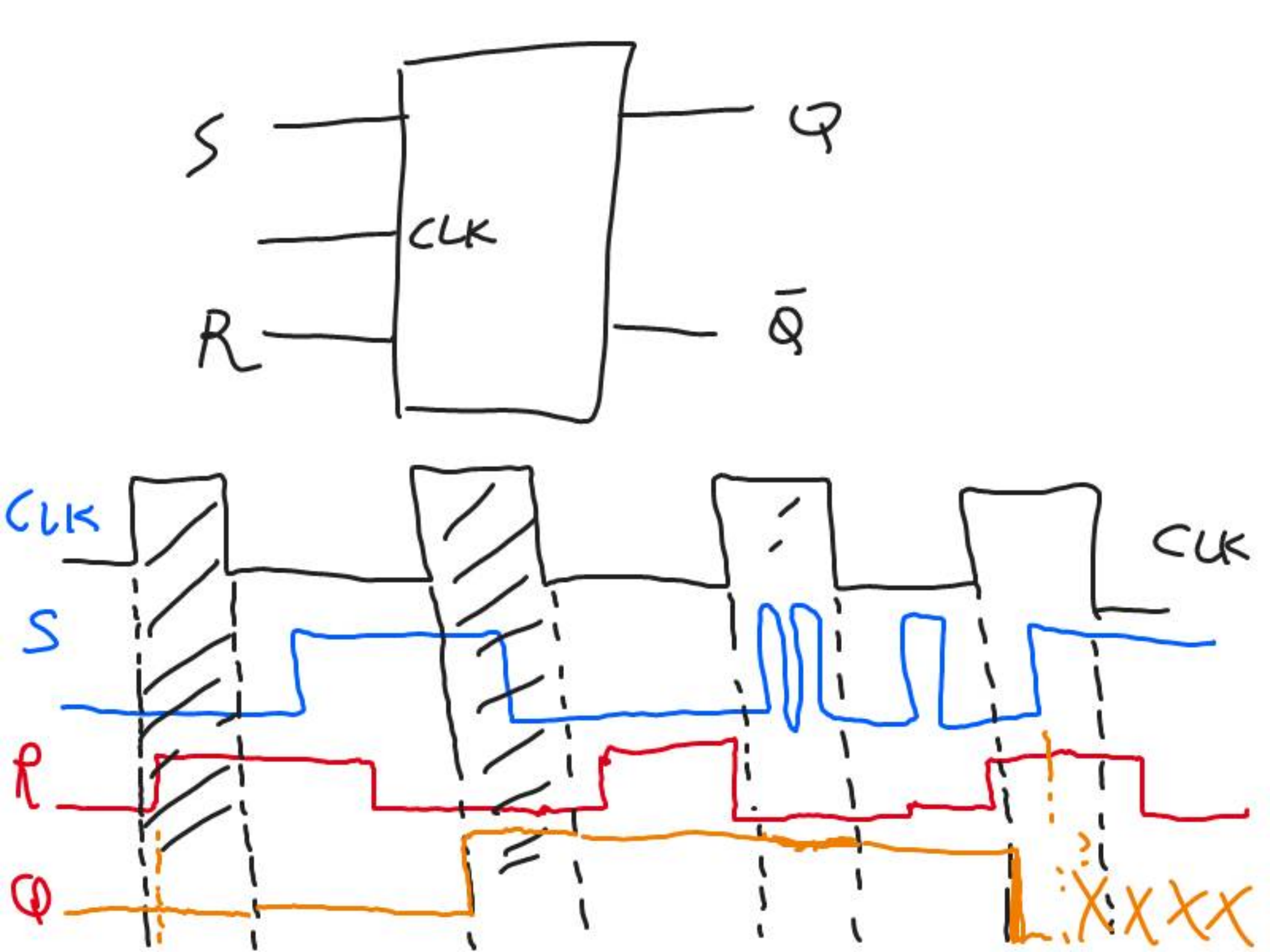
14.04.2011



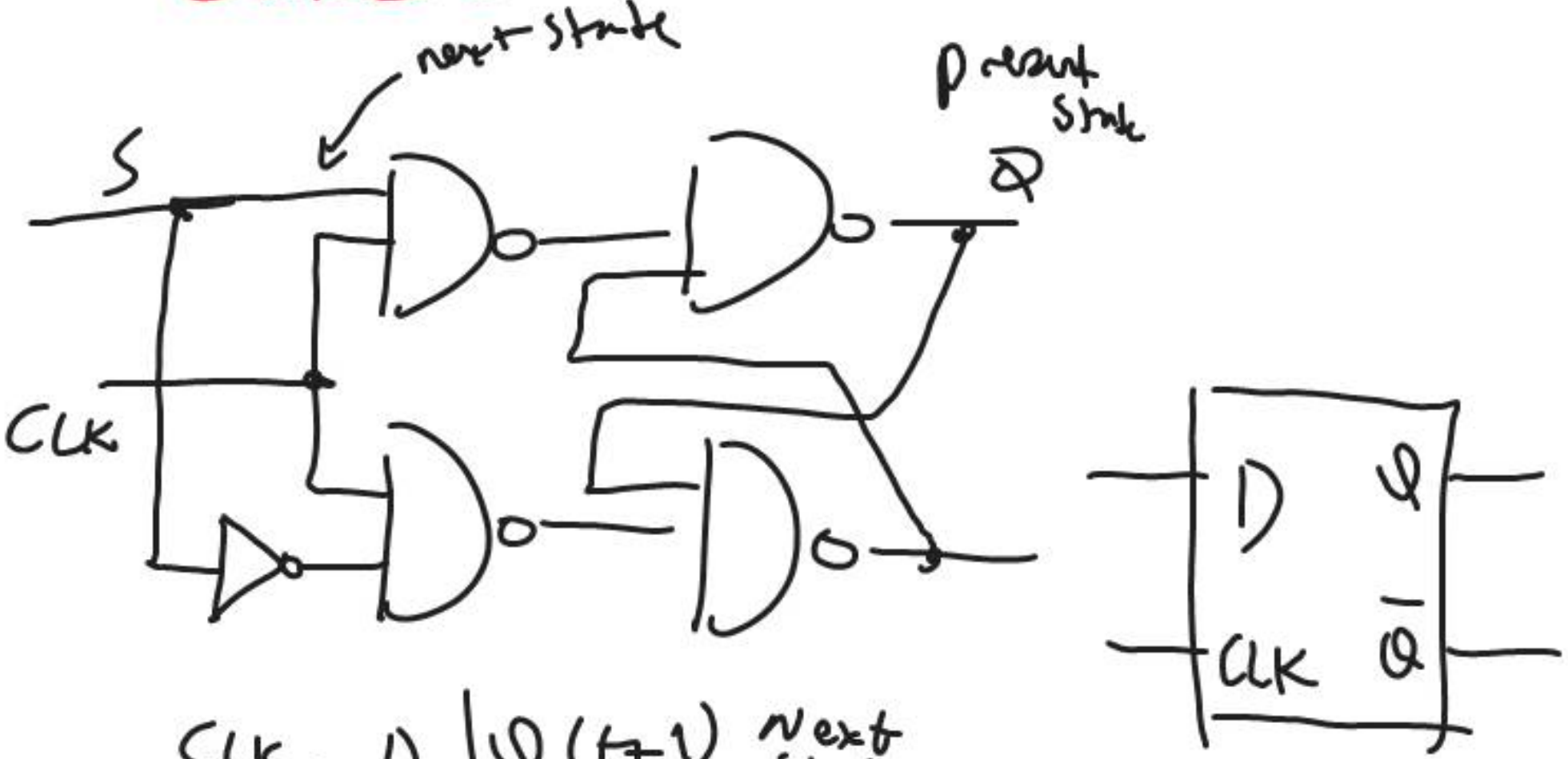
synchronized with the Clock

CLK	S	R	Next state Q(t+1)
0	X	X	Q(t) NC
1	0	0	Q(t) NC
1	0	1	0
1	1	0	1
1	1	1	X

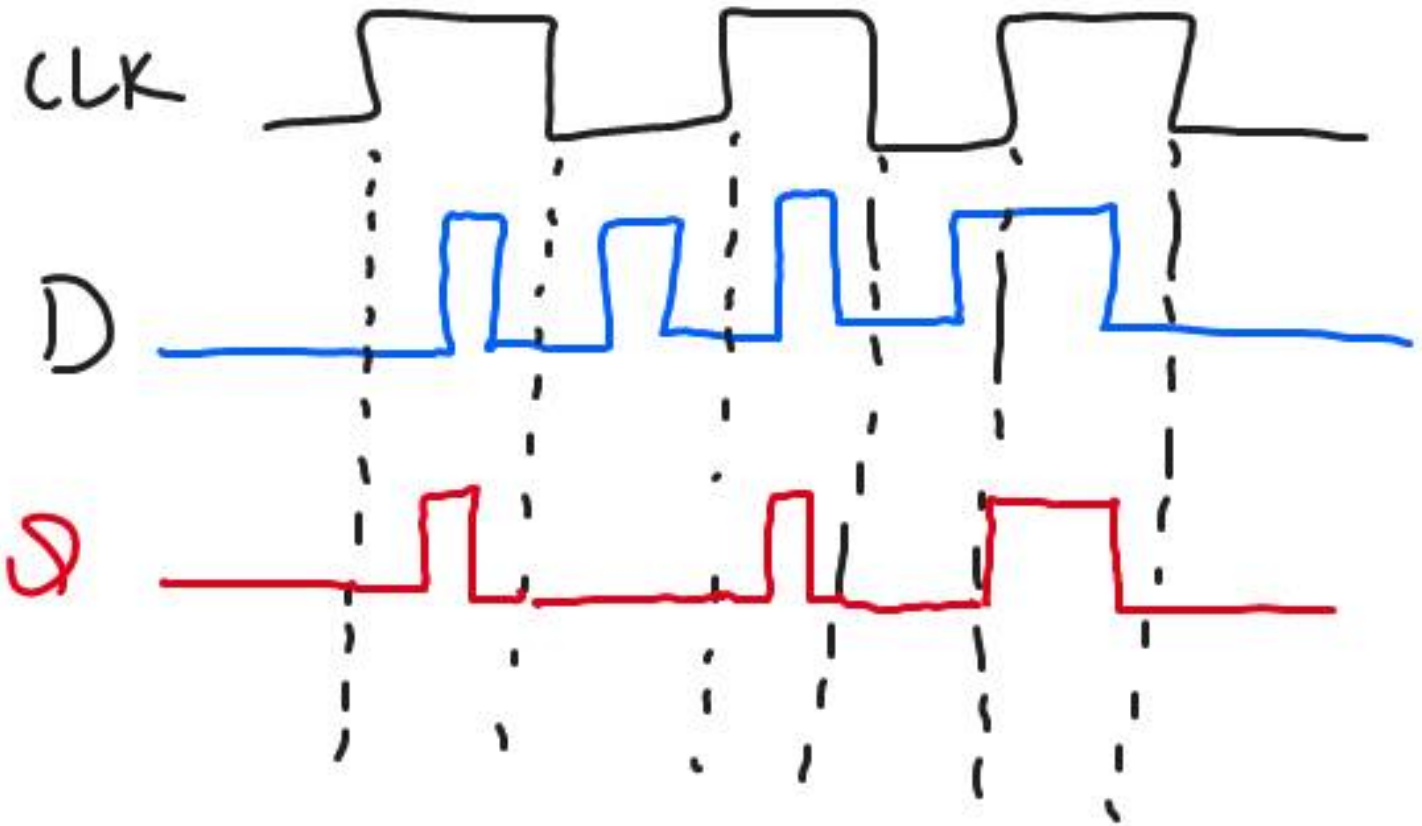
NC = No change


S
CLK
R
Q
$\bar{Q}$
CLK
CLK
S
R
Q
XXXX

Gated D Latch

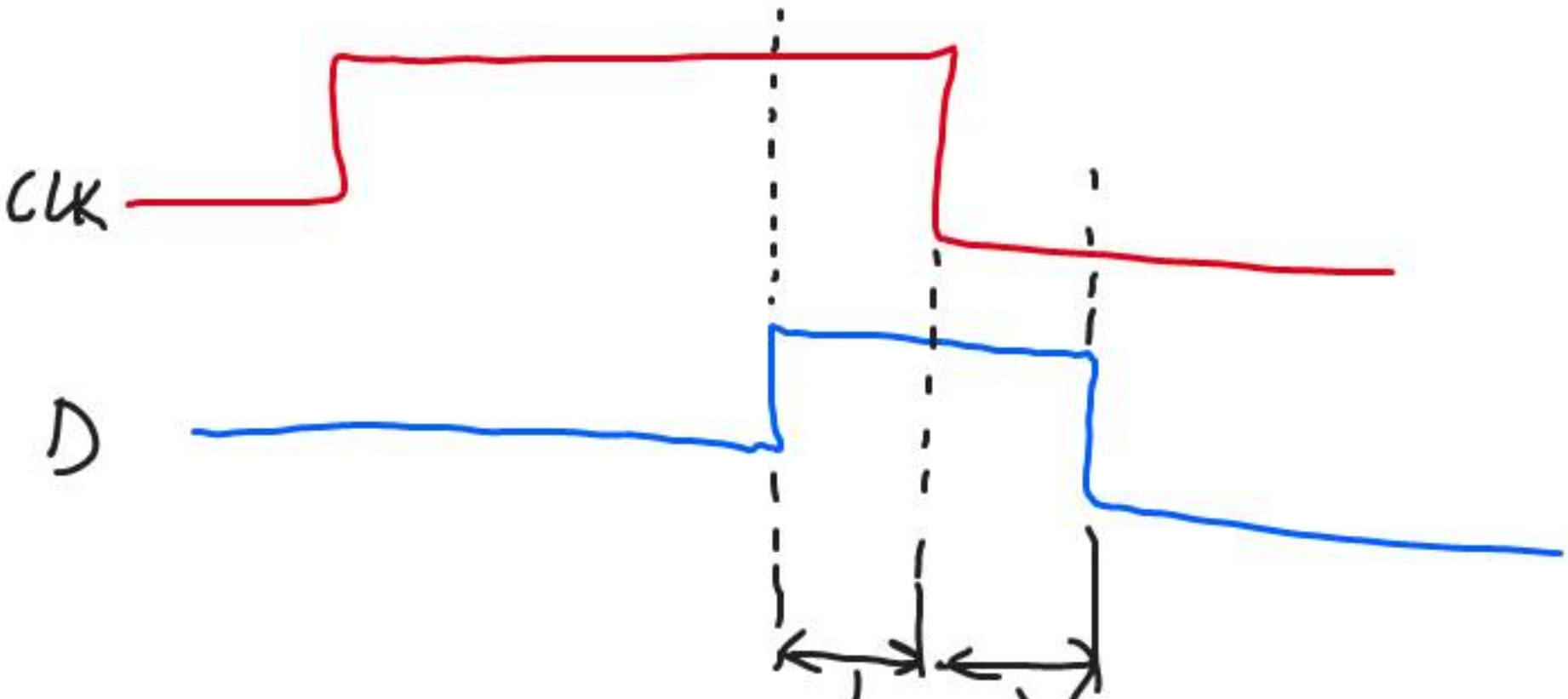


CLK	D	Q(t+1) next state
0	X	Q(t) present state
↓	0	0
1	1	1



The latch is level sensitive
(when CLK is $\overline{0}$ active cycle)

Propagation Delays

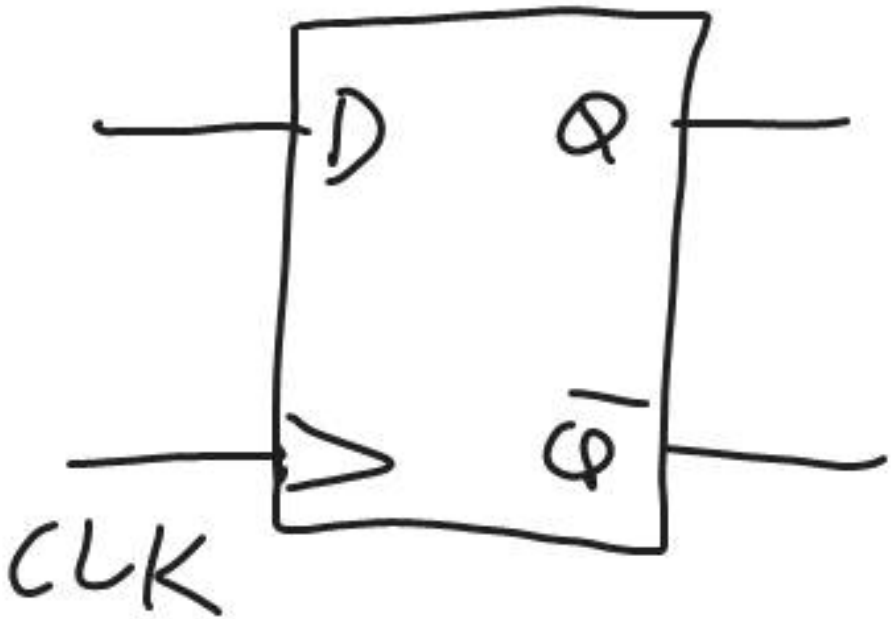


Set-up time: t_{su} t_h : hold time

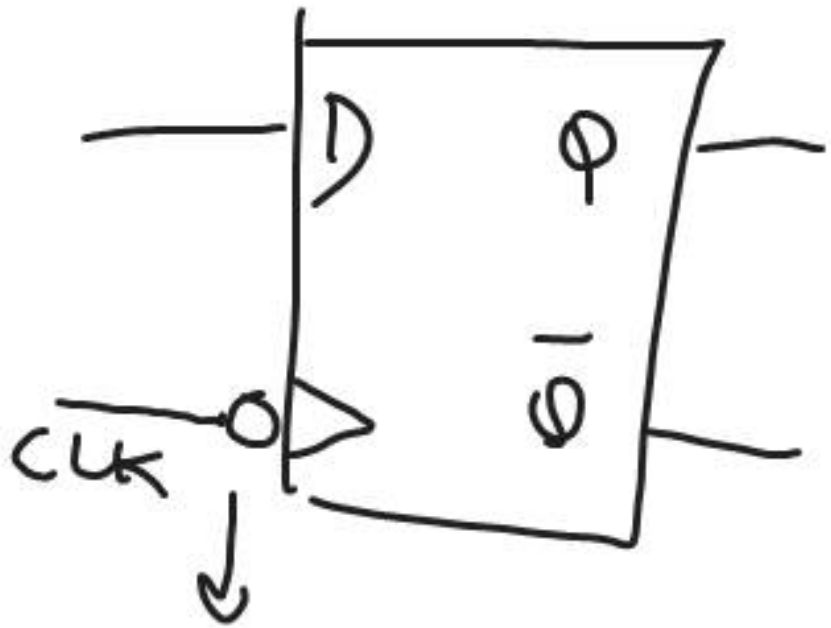
CMOS Tech. — $t_{su} = 3ns$ $t_h = 2ns$

Edge Flip Flops

Sensitive

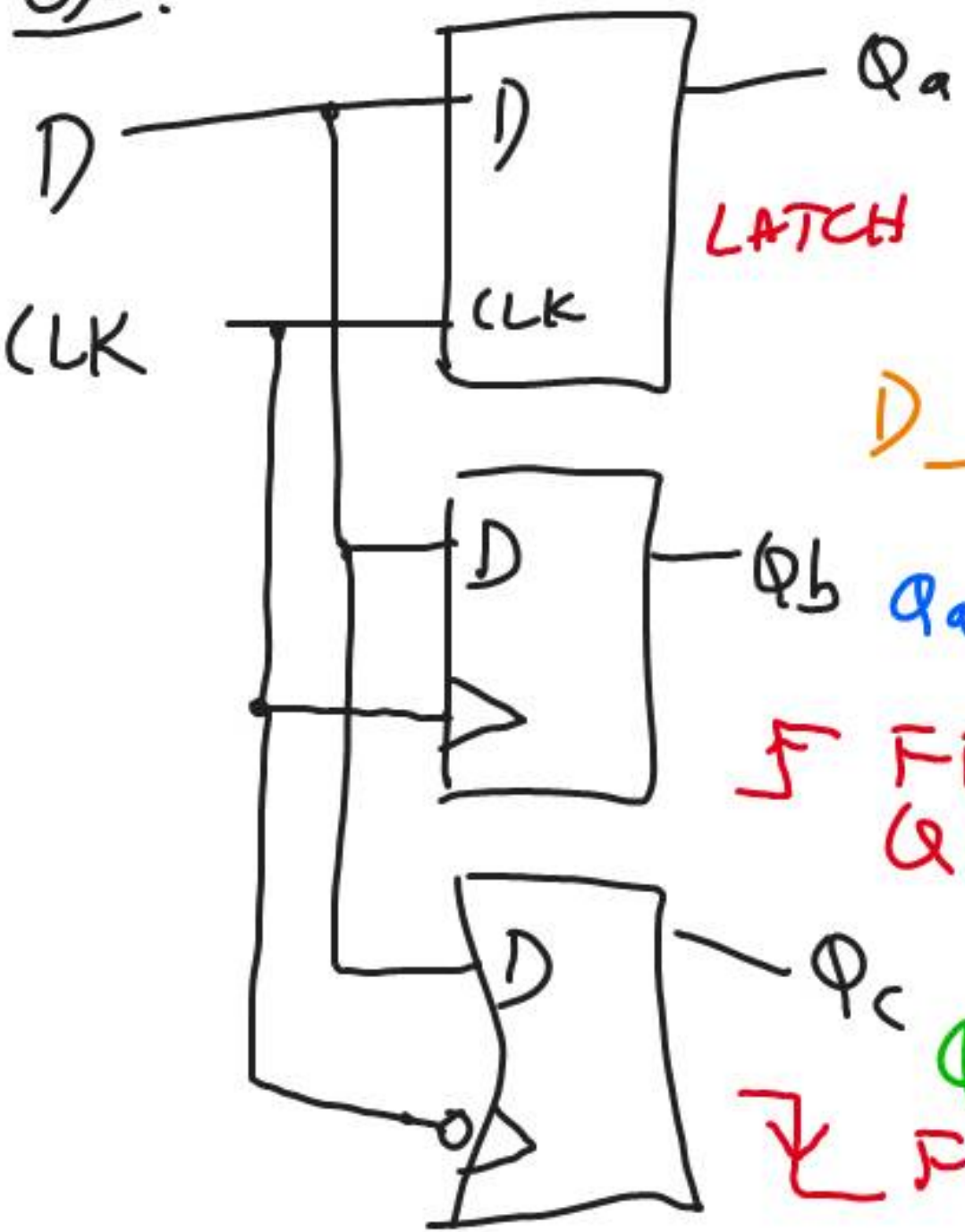


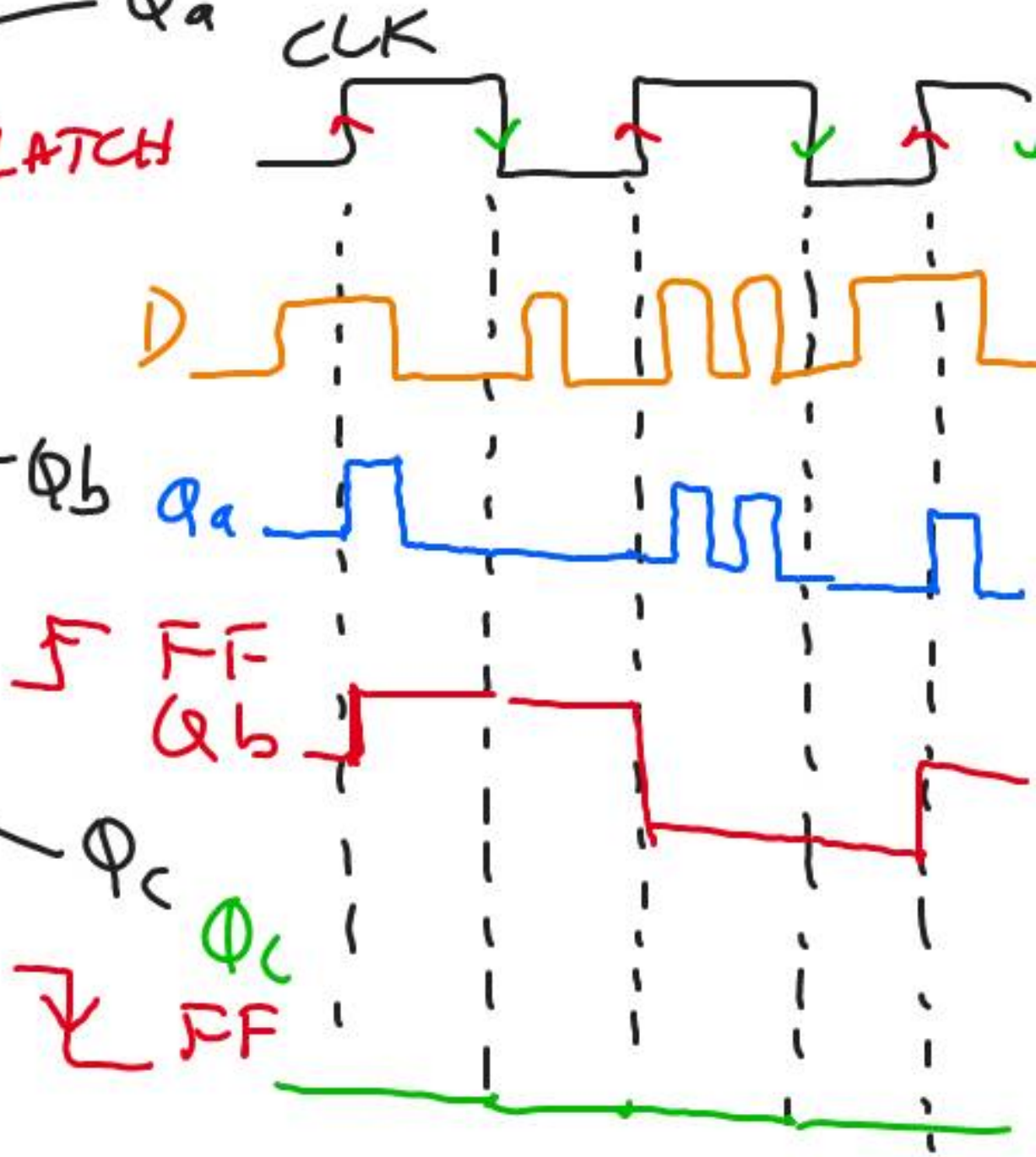
positive edge-sensitive D Flip Flop (FF)



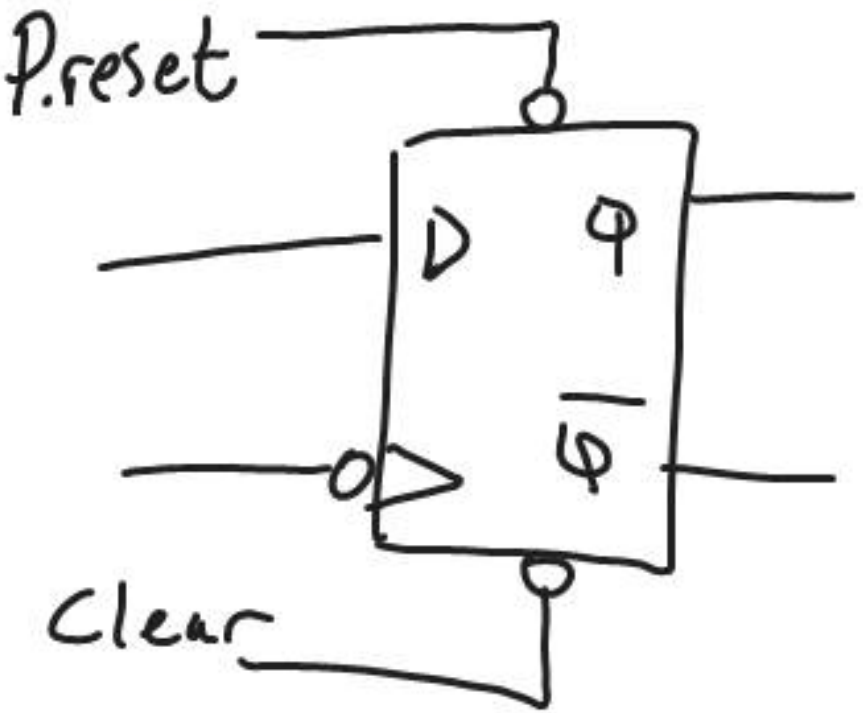
negative edge-sensitive D FF

ex:

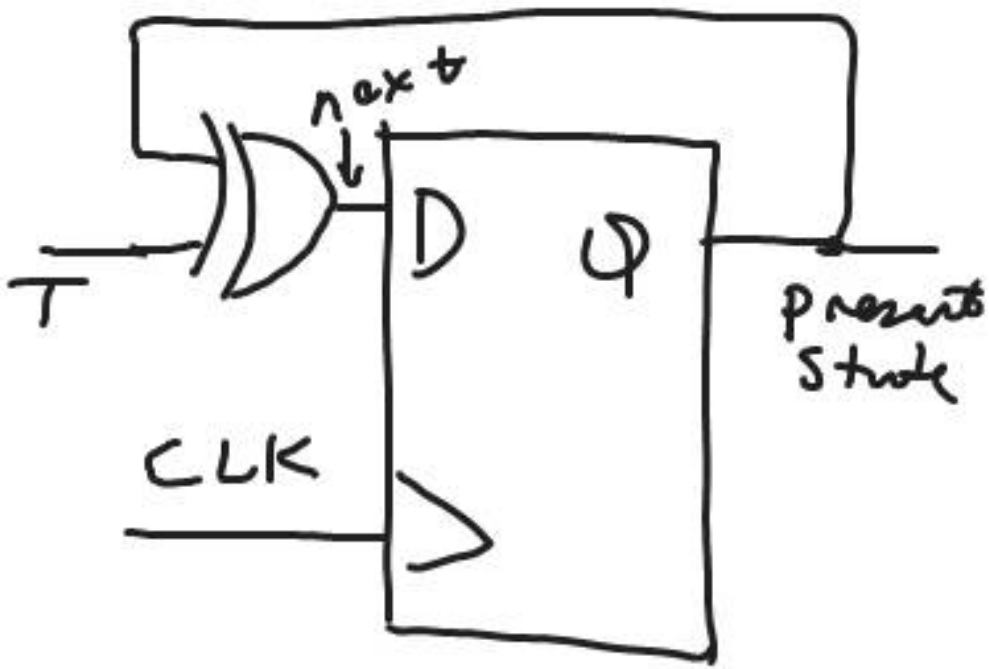




D FF with Clear and Reset



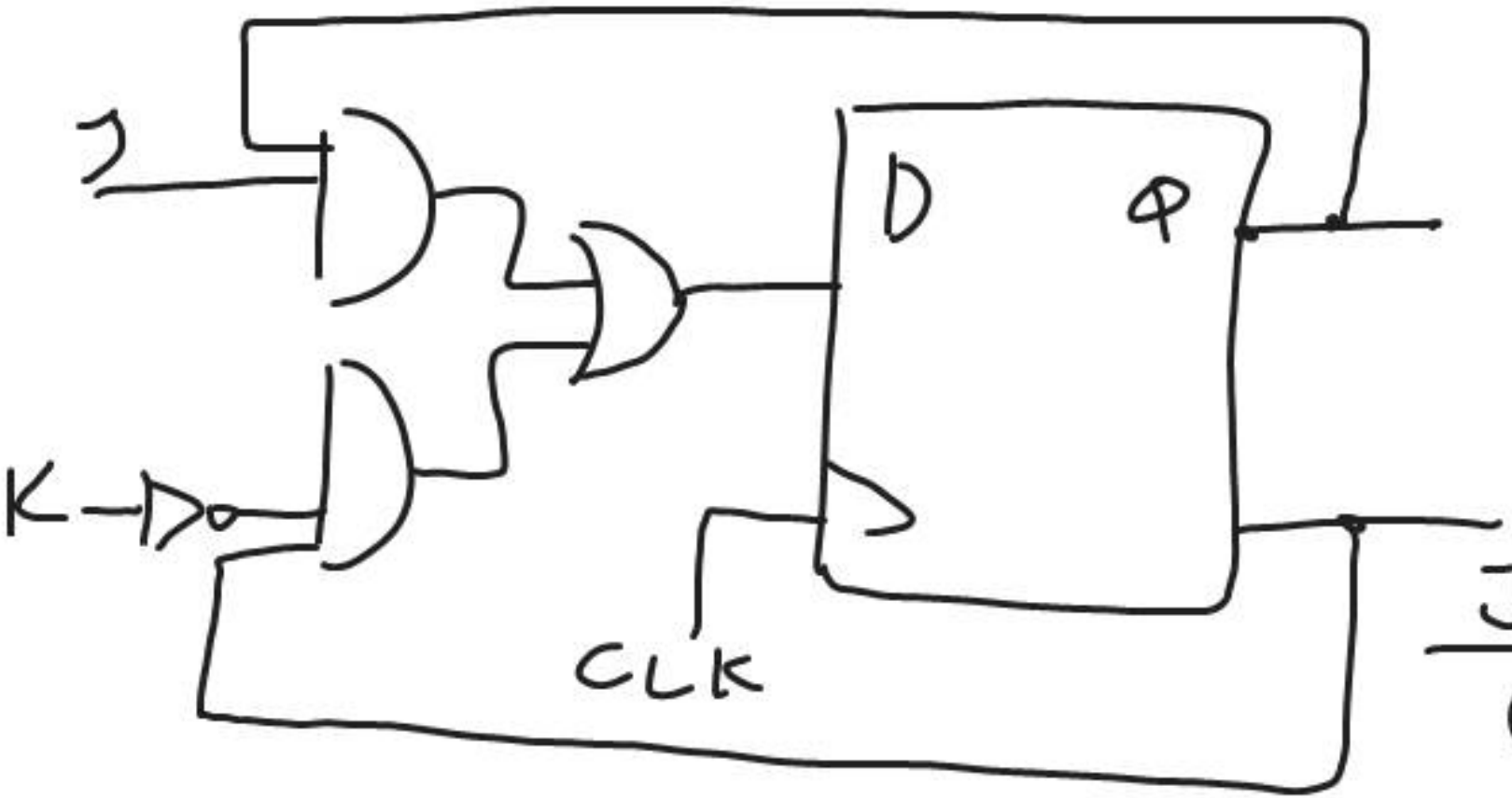
T - Flip Flop



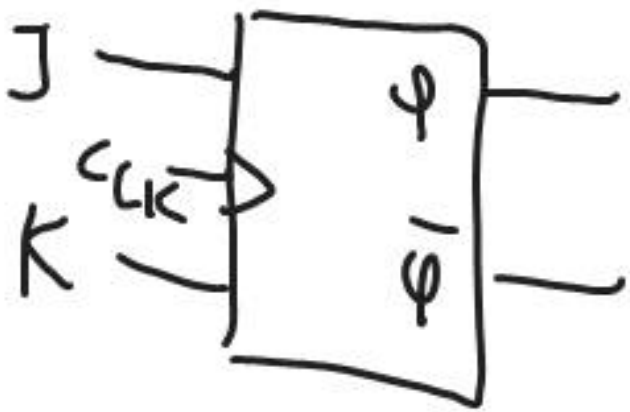
T	Q(t+1)
0	Q(t)
1	$\bar{Q}$(t)

$$Q(t+1) = T \oplus Q(t)$$

JK FLIP FLOP

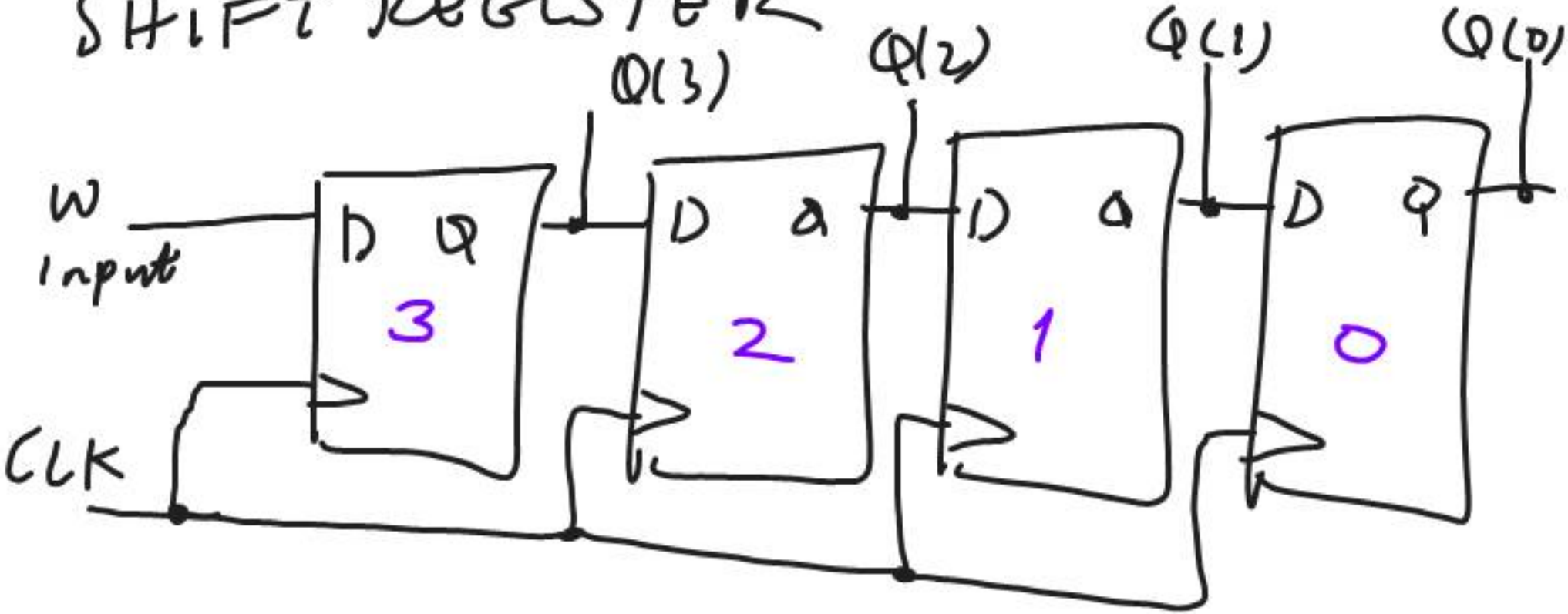


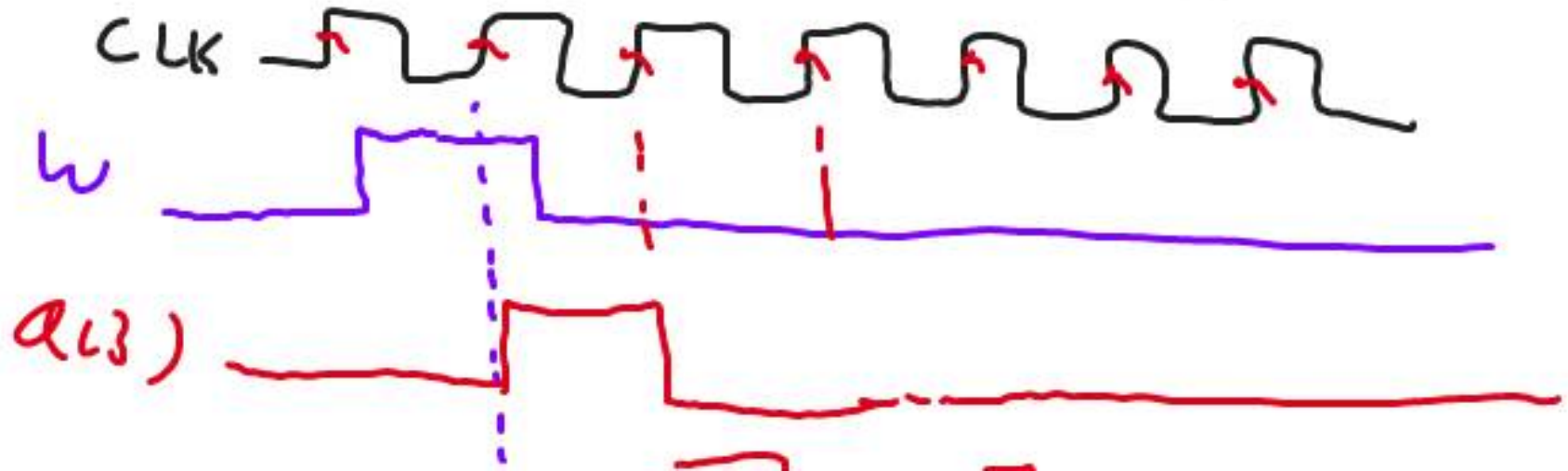
J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\overline{Q(t)}$



REGISTERS

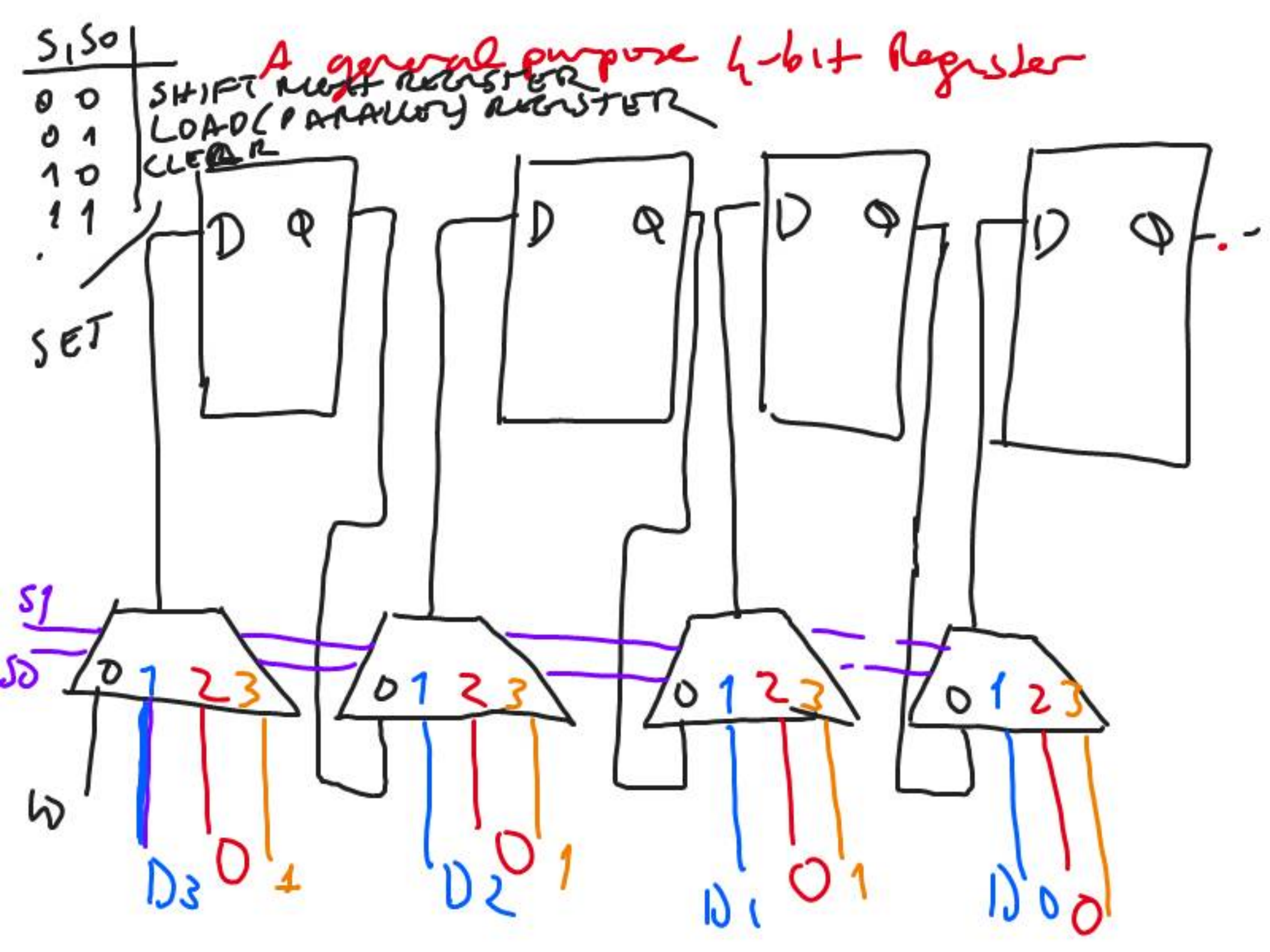
SHIFT REGISTER





A general purpose 4-bit Register

S_1 S_0	
0 0	SHIFT RIGHT REGISTER
0 1	LOAD (PARALLEL) REGISTER
1 0	CLEAR
1 1	



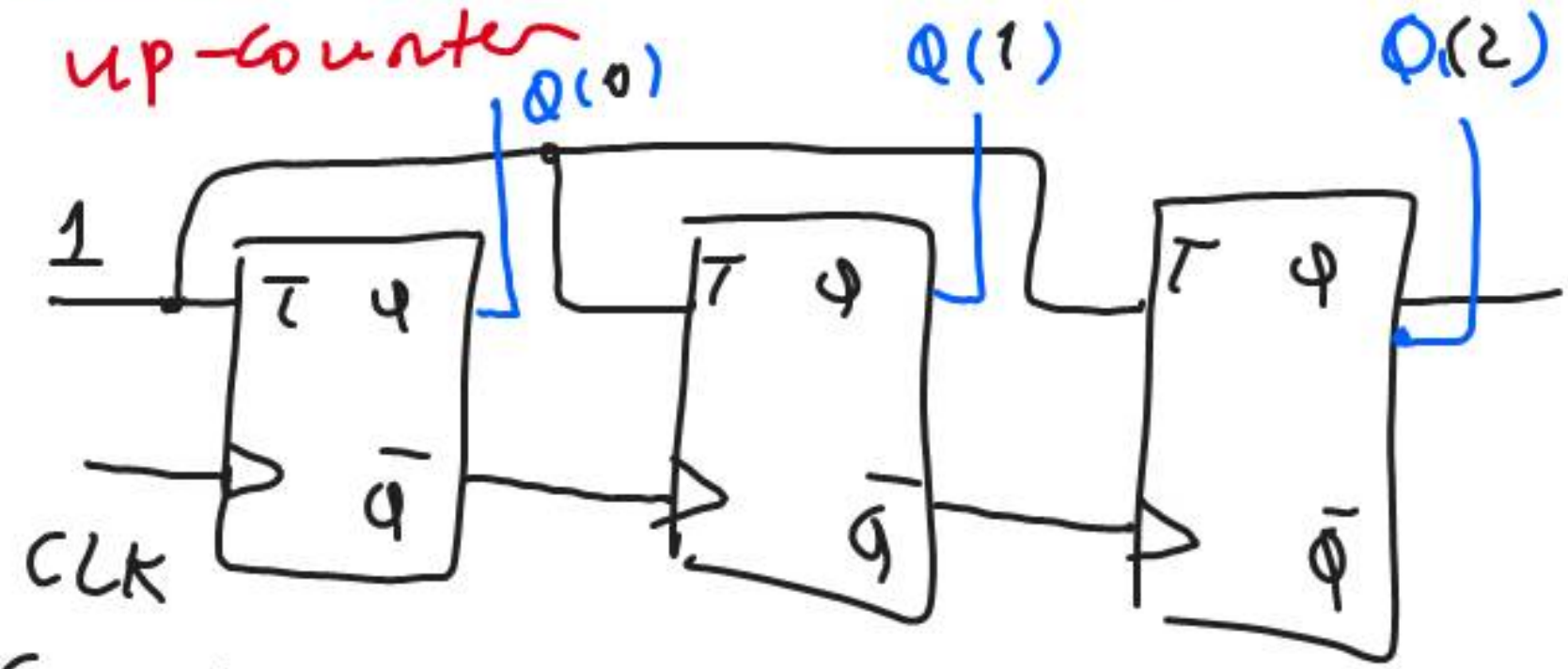
COUNTERS

Asynchronous Counters

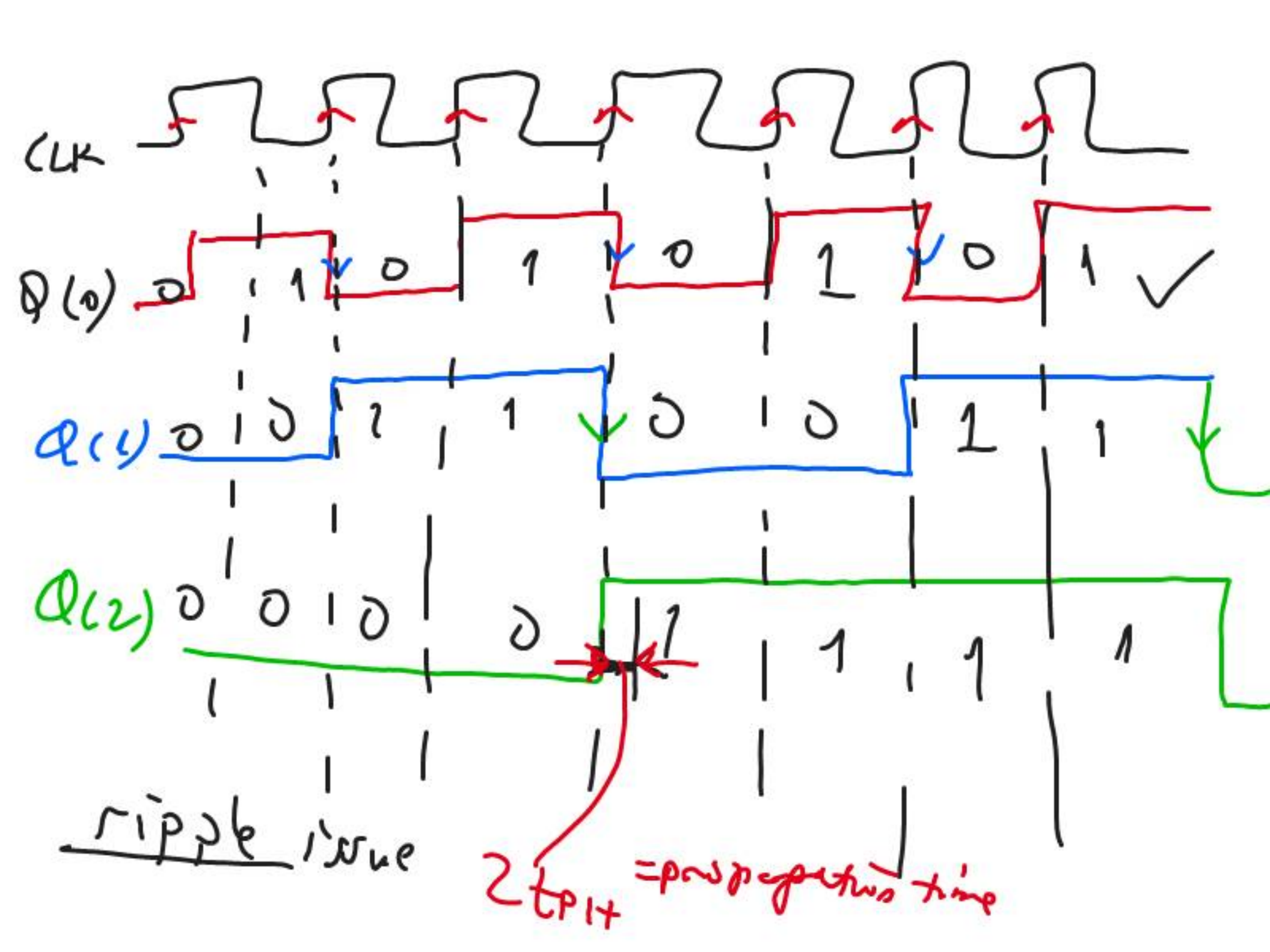
Synchronous Counters

ASYNCHRONOUS COUNTERS

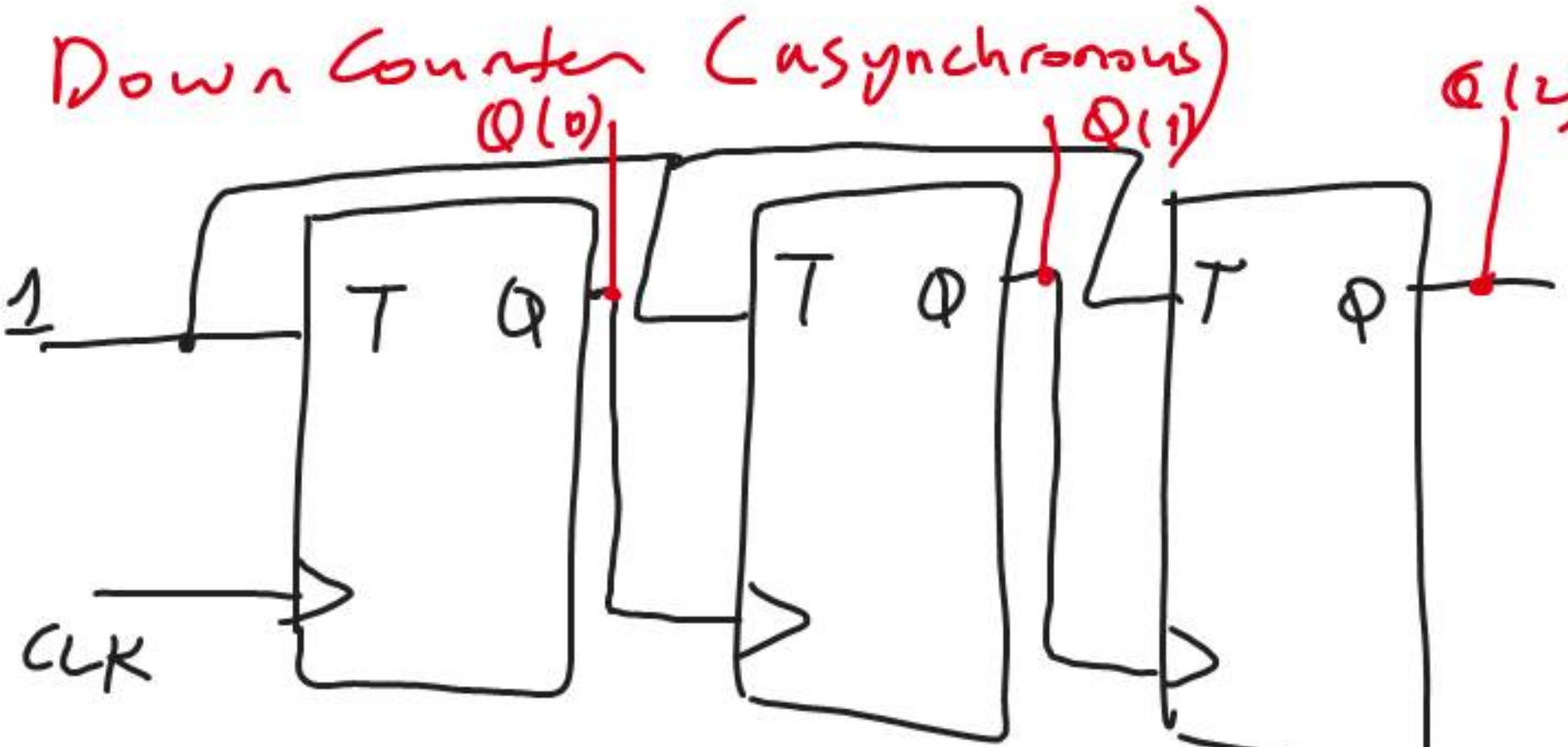
up-counter



Since CLK is not applied all the FFs at the same time this is an ASYNCHRONOUS 3-bit binary counter.


CLK
Q(0)
Q(1)
Q(2)
ripple issue
2 tpLH = propagation time

Down Counter (asynchronous)



1	1	1
1	1	0
1	0	1
1	0	0
0	1	1
0	1	0
0	0	1
0	0	0