A 4-to-16 Decoder

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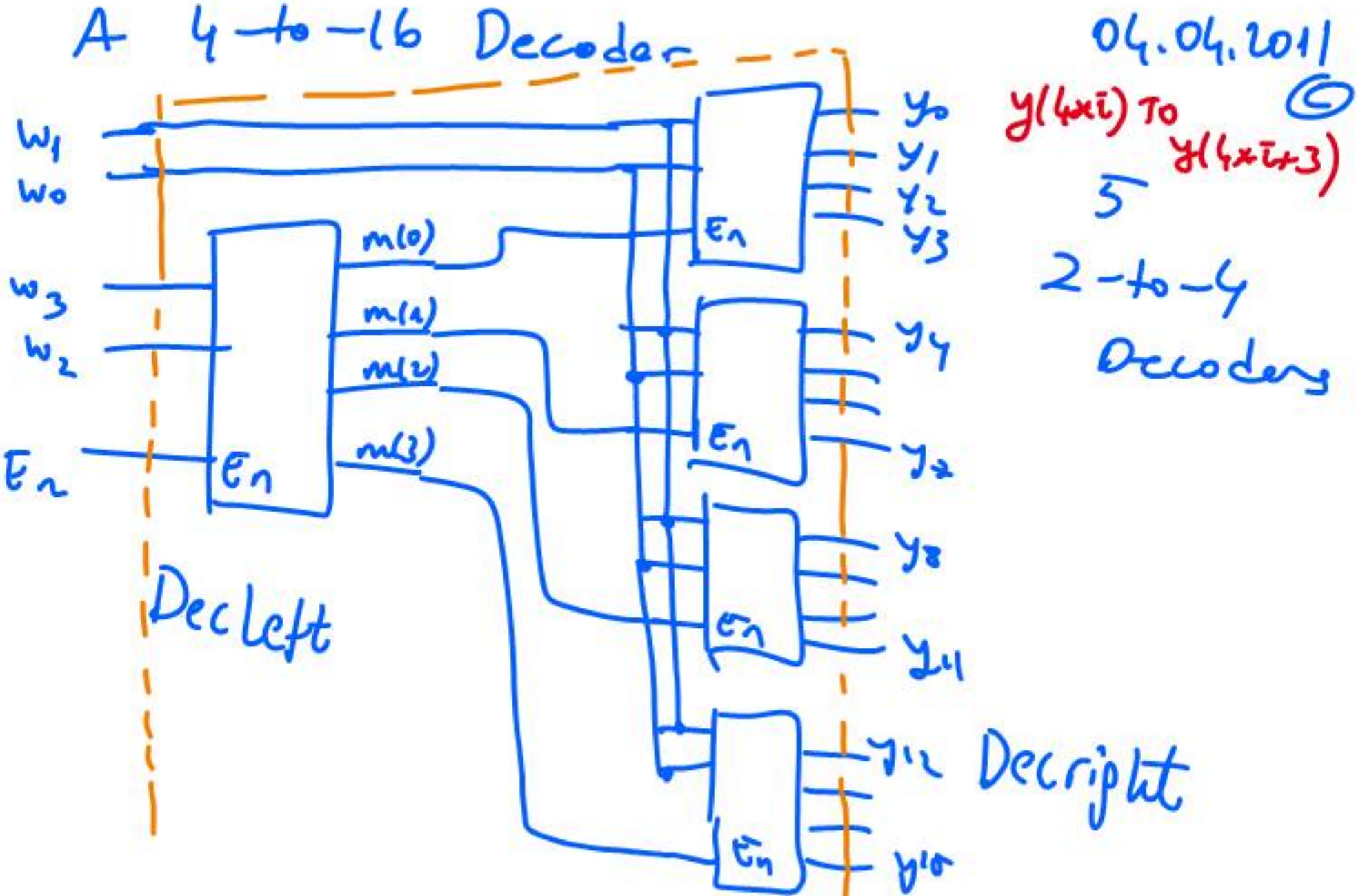

y(4xi) to y(4xi+3)

5

2-to-4 Decoders

VHDL (Structural) code for the 4-to-16 Decoder by using the 2-to-4 Dec as component.

```
Library ieee,
USE ieee.std_logic_1164.all;
ENTITY Dec4to16 IS
PORT ( W : IN STD_LOGIC_VECTOR(3 DOWNTO 0);
       En: IN STD_LOGIC;
       y: OUT STD_LOGIC_VECTOR(0 TO 15));
END Dec4to16;
```

```
ARCHITECTURE Structure of Dec 4 to 16 IS
COMPONENT Dec 2 to 4
 PORT( W: IN  STD_LOGIC_VECTOR (1 DOWN TO 0);
       En: IN  STD_LOGIC;
       y: OUT STD_LOGIC_VECTOR(0 TO 3);
 END COMPONENT;
 SIGNAL m: STD_LOGIC_VECTOR(0 TO 3);
 BEGIN
```

* FOR GENERATE

G1: FOR i IN 0 TO 3 GENERATE

DECRIGHT : DEC 2 TO 4 PORT MAP (

w(1 DOWNTO 0), m(i), y(4*i TO 4*i+3));

En

* IF GENERATE

G2: IF i=3 GENERATE

DECLEFT : DEC 2 TO 4 PORT MAP (w(i DOWNTO i-1),

En, n);

END GENERATE;
END GENERATE;
END STRUCTURE;

SEQUENTIAL ASSIGNMENT STATEMENTS

* IF-THEN-ELSE Statement
* CASE Statement

They are always enclosed in a PROCESS Statement &

- f ∈ W0 when S = '0' else f ∈ W1

SELECT:

WITH S SELECT

f ∈ W0 WHEN '0'

f ∈ W1 WHEN OTHERS;

Remind: Concurrent statements.

A 2-to-1 mux: ex write VHDL using sequential code

using IF-THEN-ELSE Statement

```
ARCHITECTURE Behavior of 2 to 1 mux is
BEGIN
  PROCESS (w0, w1, s)        -- sensitivity list of the PROCESS
  BEGIN
    IF s = '0' THEN
      f <= w0;
    ELSE
      f <= w1;
    END IF;
  END PROCESS;
END Behavior;
```

Some example with a CASE statement:

mux-2-to-1 in CASE

```
:
ARCHITECTURE Behavior of MUX2TO1 IS
BEGIN
PROCESS (W0, W1, S)
BEGIN
CASE S IS
  WHEN '0' =>
    f <= W0;
  WHEN OTHERS
    f <= W1;
END CASE;
END PROCESS;
END Behavior;
```

ex :

```
PROCESS (w0, w1, s)
BEGIN
f <= w0 ;
IF s = '1' THEN
 f <= w1;
 END IF;
END PROCESS;
END BEHAVIOR;
```

← by using a default assignment.