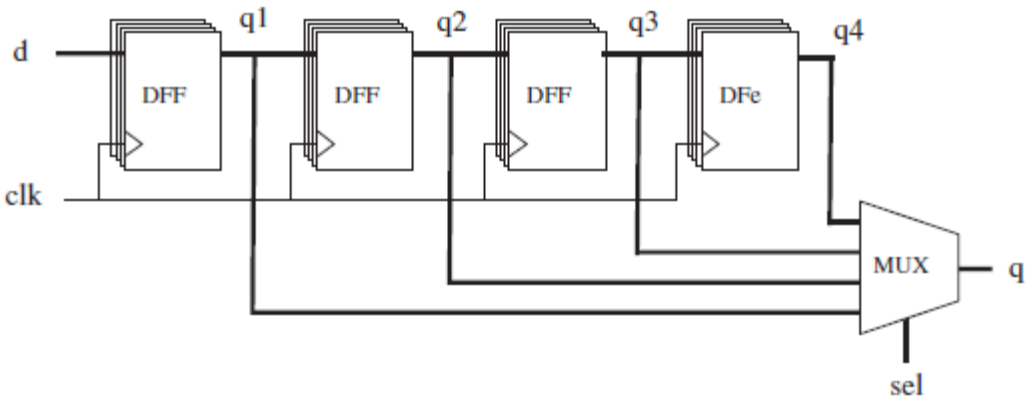
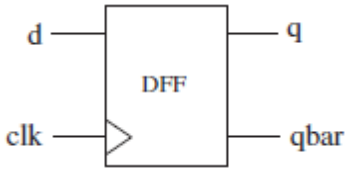
ECE 477 HW1 Due 26 December-2016

Q1) Figure below shows the diagram of a programmable data delay circuit. The input (d) and output (q) are 4-bit buses. Depending on the value of sel (select), q should be one, two, three, or four clock cycles delayed with respect to d.

(a) Write a VHDL code for this circuit;
(b) How many flip-flops do you expect your solution to contain?
(c) Synthesize your solution and open the report file. Verify whether the actual number of flip-flops matches your prediction.



Q2) For the D flip flop given in the figure below you are asked to examine each of the solutions below and determine whether q and qbar will work properly. Briefly explain your answers.

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ENTITY dff IS
PORT ( d, clk: IN BIT;
          q, qbar: BUFFER BIT);
END dff;
-------- Solution 1 ----------------
ARCHITECTURE arch1 OF dff IS
        SIGNAL temp: BIT;
        BEGIN
        PROCESS (clk)
                BEGIN
                        IF (clk'EVENT AND clk='1') THEN
                        temp <= d;
                        q <= temp;
                        qbar <= NOT temp;
                        END IF;
                END PROCESS;
END arch1;
```

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-------- Solution 2 -------------------
ARCHITECTURE arch2 OF dff IS
        SIGNAL temp: BIT;
        BEGIN
        PROCESS (clk)
                BEGIN
                        IF (clk'EVENT AND clk='1') THEN
                        temp <= d;
                        END IF;
                        q <= temp;
                        qbar <= NOT temp;
                END PROCESS;
        END arch2;

-------- Solution 3 -------------------
ARCHITECTURE arch3 OF dff IS
        SIGNAL temp: BIT;
        BEGIN
        PROCESS (clk)
                BEGIN
                IF (clk'EVENT AND clk='1') THEN
                temp <= d;
                END IF;
        END PROCESS;
        q <= temp;
        qbar <= NOT temp;
END arch3;
---------------------------------------
```

Q3) For the D flip flop in the previous question You are asked to examine each of the solutions below and determine whether q and qbar will work as expected. Briefly explain your answers.

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ENTITY dff IS
PORT ( d, clk: IN BIT;
q: BUFFER BIT;
qbar: OUT BIT);
END dff;

-------- Solution 1 -------------------
ARCHITECTURE arch1 OF dff IS
BEGIN
        PROCESS (clk)
        VARIABLE temp: BIT;
        BEGIN
                IF (clk'EVENT AND clk='1') THEN
                        temp := d;
                        q <= temp;
```

```
                        qbar <= NOT temp;
                END IF;
        END PROCESS;
END arch1;

-------- Solution 2 --------------------
ARCHITECTURE arch2 OF dff IS
BEGIN
        PROCESS (clk)
        VARIABLE temp: BIT;
        BEGIN
                IF (clk'EVENT AND clk='1') THEN
                temp := d;
                q <= temp;
                qbar <= NOT q;
                END IF;
        END PROCESS;
END arch2;

-------- Solution 3 --------------------
ARCHITECTURE arch3 OF dff IS
BEGIN
        PROCESS (clk)
        VARIABLE temp: BIT;
        BEGIN
                IF (clk'EVENT AND clk='1') THEN
                temp := d;
                q <= temp;
                END IF;
        END PROCESS;
qbar <= NOT q;
END arch3;
---------------------------------------
```